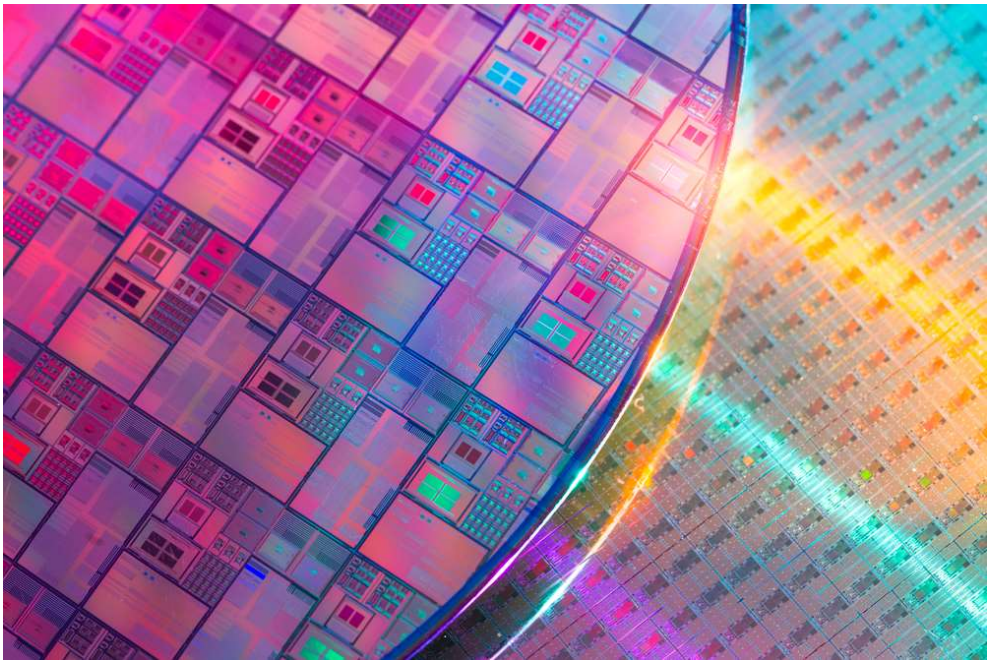
UNIVERSITY OF WEST ATTICA FACULTY OF ENGINEERING DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Diploma Thesis

Design and Simulation of CMOS Analog IC building blocks and operational amplifiers



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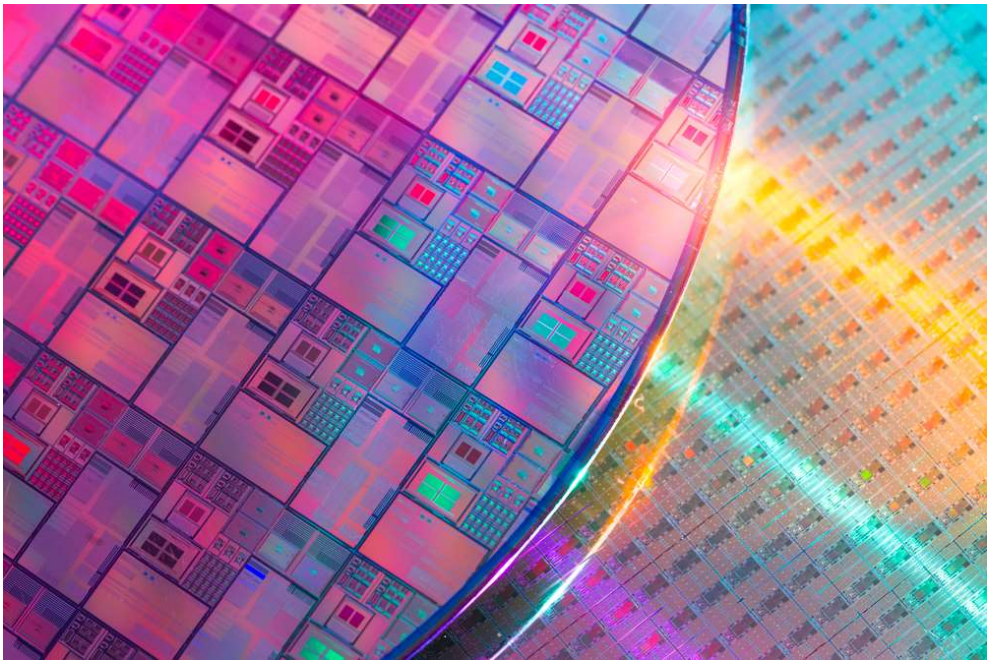
ATHENS-EGALEO, May 2023

ΠΑΝΕΠΙΣΤΗΜΙΟ ΔΥΤΙΚΗΣ ΑΤΤΙΚΗΣ ΣΧΟΛΗ ΜΗΧΑΝΙΚΩΝ ΤΜΗΜΑ ΗΛΕΚΤΡΟΛΟΓΩΝ & ΗΛΕΚΤΡΟΝΙΚΩΝ ΜΗΧΑΝΙΚΩΝ

Διπλωματική Εργασία

Σχεδίαση και προσομοίωση αναλογικών ολοκληρωμένων κυκλωμάτων CMOS δομικών στοιχείων και τελεστικών ενισχυτών



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Επιθυμώ την απαγόρευση πρόσβασης στο πλήρες κείμενο της εργασίας μου μέχρι …… και έπειτα από αίτησή μου στη Βιβλιοθήκη και έγκριση του επιβλέποντος/ουσας καθηγητή/ήτριας.»

Ο/Η Δηλών/ούσα
(Αποστολάτος Νικήτας)

I would like to thank Professor George Patsis for the guidance and support he provided during the writing of my thesis.

I am also thankful to my family and friends for their support all those years of my studies.

ABSTRACT

In this thesis, it will be briefly discussed the behaviour of CMOS transistors, the physical design of integrated passive components and finally design the basic building blocks and operational amplifiers.

For simulations and calculations the software used is Tanner EDA (Mentor Graphics) and MATLAB.

Analog systems consist of basic cells and passive components. Basic cells are operational amplifiers and comparators. They are constructed from simple gain stages and differential pairs. These provide gain, buffering and mixing and can be used in almost any applications.

DC and AC analysis for understanding the behaviour he various designed circuits is presented in the following chapters.

KEYWORDS

CMOS, integrated circuits (ICs), resistors, capacitors, transistors, switches, building blocks, push-pull inverter, inverter with active load, cascode with active load, cascode with cascode load, differential amplifier, CMOS operational amplifiers, single stage mirrored cascode OTA, two stage operational amplifier.

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LIST OF ABBREVIATIONS

CMOS: Complementary metal-oxide semiconductor

OTA: Operational transconductance amplifier

NMOS: N-type metal oxide semiconductor

PMOS: P-type metal oxide semiconductor

IC: Integrated circuit

INTRODUCTION

In every IC circuit around us always exists an analog and a digital part.

Analog IC circuits are important in applications such as amplification, power management, filtering and signal processing.

In this thesis, we examine amplification circuits. Specifically operational amplifiers.

THESIS STATEMENT

The purpose of this thesis is to present the basic structures that take place in analog circuits. These structures have been made based on SPICE models. They designed and verified following the most common design steps. The reader can find information from the behaviour of the transistors, the implementation of passive components and the design of operational amplifiers.

AIMS AND OBJECTIVES

This thesis presents analog circuit design concepts.

Given performance specifications we develop, modify and design the active and passive components of the circuits.

METHODOLOGY

SPICE models for transistors and passive components are used.

From the schematic circuit analysis the correct circuit operation according to specifications is verified

Physical design (layout) follows.

LVS (Layout vs Schematic) checks are used to match the performance specifications.

INNOVATION

One of the innovative aspects of this thesis is to design unique building blocks and operational amplifier circuits based on 0.35μm technology following some performance specifications. In every circuit follows the designing process to understand how these blocks are designed. Usually building blocks such as operational amplifiers consist of many transistors. For someone with little experience it becomes difficult to start and design these kind of blocks. It is not possible to use equations and calculate every parameter for this big circuits. A designer uses in many cases SPICE simulations to evaluate the results. In this thesis they are presented some ways of thinking in order to design these kind of building blocks.

STRUCTURE

In this thesis we have four different chapters. In the first chapter we study the fabrication of NMOS and PMOS transistor but more specifically the diode configuration. Performing specific simulations to extract basic characteristics that are useful for designing and understanding how transistors work.

In the second chapter are mentioned specific ways of fabricating IC resistors and capacitors. Deals with problem of switching especially with charge injection and how this problem can be solved.

Third chapters is for building blocks. There are mentioned different ways of designing building blocks that are used as amplifiers.

Operational amplifiers described on fourth chapter. They are designed to fulfil some performance specifications.

1 Schematic and Layout behaviour of NMOS and PMOS transistor

On this chapter we will simulate and analyse the behaviour of NMOS and PMOS transistors.

1.1 NMOS transistor structure

The NMOS (N-type Metal Oxide Semiconductor) transistor can be fabricated on a P-type substrate also called as bulk. The device consists of two heavily-doped regions implanted with N-type material. This results in the forming of two regions also called as source and drain. Gate is a heavily-doped and conductive material consisting of a polysilicon layer. All the useful action of the device happens between the two terminals and the gate.

1.1.1 Schematic Design

On S-edit we setup the dc voltages VGS and VDS as parameters in the program. Using NMOS transistor with aspect ratio 10 and technology 0.35μm (Fig. 1). We use the SPICE model described on SPICE files section 5.2.

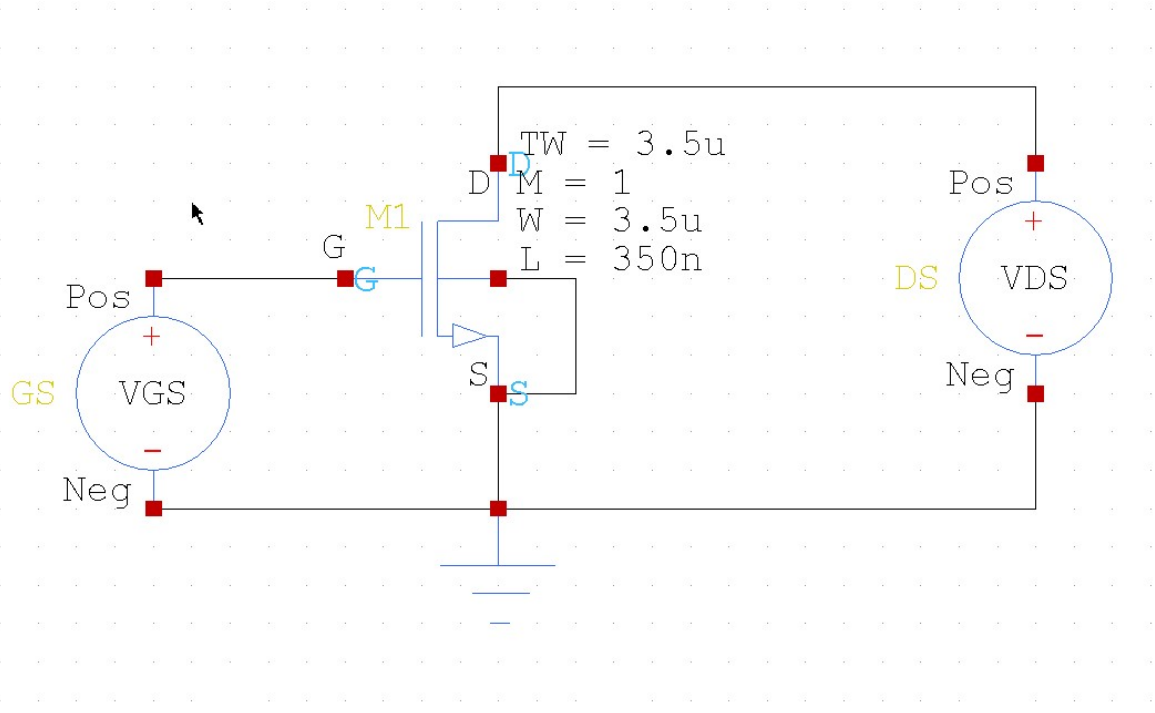


Figure 1: NMOS schematic design.

1.1.2 Layout Design

Using L-edit NMOS is fabricated on the substrate with N_Implant layer for the drain and source. On top of N_Implant a layer called Active defines the area of the transistor called width (W). The gate of the transistor made with Poly layer and the bulk consists of P_Implant with active on top. Contacts sit on top of a metal1 layer to achieve the connections between layers. Figure 2 shows the layout structure of the NMOS transistor. Figure 3 shows the cross section of the NMOS transistor.

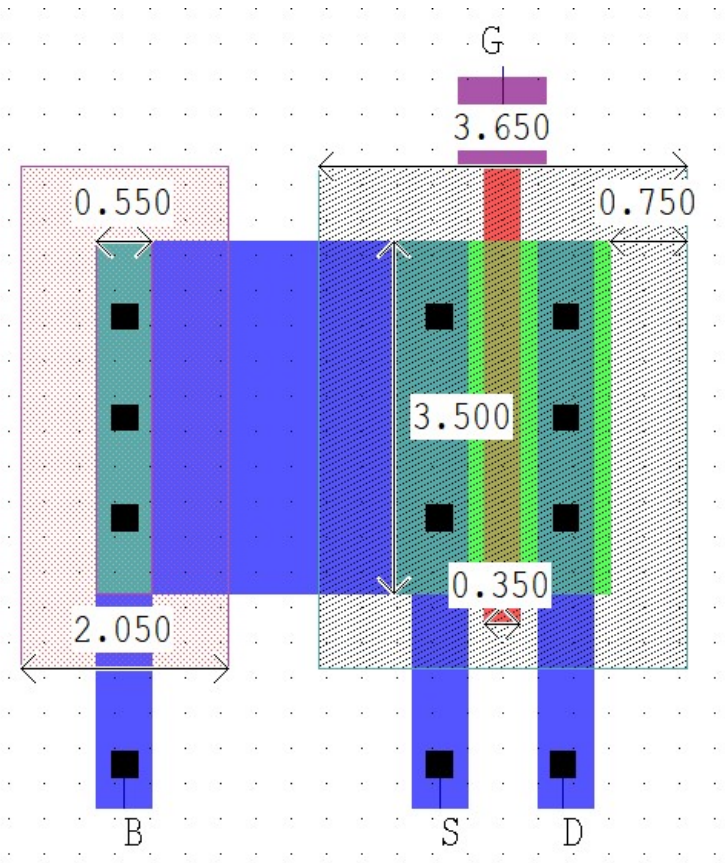


Figure 2: NMOS layout design.

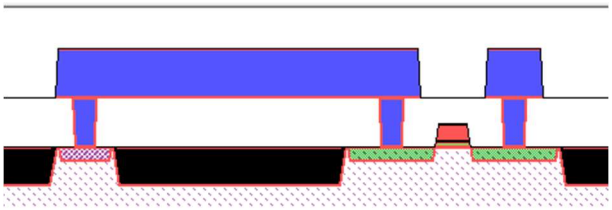


Figure 3: Cross-section of NMOS transistor.

1.1.3 Verification Layout vs Schematic

After the fabrication of layout and the schematic design we use the extract tool in order to obtain the netlist for the transistors. We use the LVS (Layout vs Schematic) tool to compare the netlists of the schematic (Netlist 1) and layout (Netlist 2) and verify that are equal (Fig. 4 and 5).

```
* SPICE export by:  S-Edit 2019.2.0
* Export time:     Sun Mar 12 16:43:44 2023
* Design path:     C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\lib.defs
* Library:         DESIGNS
* Cell:           Cell_PMOS
* Testbench:       Spice
* View:           schematic
* Export as:       top-level cell
* Export mode:     hierarchical
* Exclude empty:    yes
* Exclude .model:   no
* Exclude .hdl:     no
* Exclude .end:     no
* Expand paths:     yes
* Wrap lines:      no
* Exclude simulator commands:  no
* Exclude global pins:        no
* Exclude instance locations:  no
* Control property name(s):    SPICE
********* Simulation Settings - General Section *********
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
********* Simulation Settings - Parameters *********
.param VGS = 3.3
.param VDS = 3.3
***** Top Level *****
MM1 D G Gnd Gnd MODN W=3.5u L=350n AS=3.15p PS=8.8u AD=3.15p PD=8.8u $ $x=4500 $y=4100
$w=400 $h=600
VDS D Gnd  DC VDS $ $x=6100 $y=4100 $w=400 $h=600
VGS G Gnd  DC VGS $ $x=3800 $y=3800 $w=400 $h=600
.PLOT    I(MM1,D) $ $x=6900 $y=4800 $w=2000 $h=400
.PLOT    gm(MM1) $ $x=6150 $y=2650 $w=3300 $h=300
********* Simulation Settings - Analysis Section *********
.op
.dc VDS 0v 3.3v 0.01 SWEEP VGS 0v 3.3v 0.6
********* Simulation Settings - Additional SPICE Commands *********
.dc lin param VGS 0v 3.3v 0.001
.end
```

Netlist 1: NMOS Schematic netlist.

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Sun Mar 12 12:52:56 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_NMOS
* Write Flat:               NO
********************************************************************************
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
.temp 25
**************************************
.param VDS=3.3
.param VGS=3.3
**************************************
M1 D G GND GND MODN l=3.5e-07 w=3.5e-06 ad=3.15e-12 as=3.15e-12 pd=8.8e-06 ps=8.8e-06  $ (13.825
18.688 14.175 22.188)
**************************************
VDS D GND VDS
VGS G GND VGS
**************************************
.dc lin param VDS 0v 3.3v 0.1v sweep VGS 0v 3.3v 0.6v
.dc lin param VGS 0v 3.3v 0.001
**************************************
.print dc i(M1,D)
.print dc gm(M1)
**************************************
* Top level device count
* M(NMOS25)                  1
* Number of devices:         1
* Number of nodes:  3
```

Netlist 2: NMOS Layout netlist.

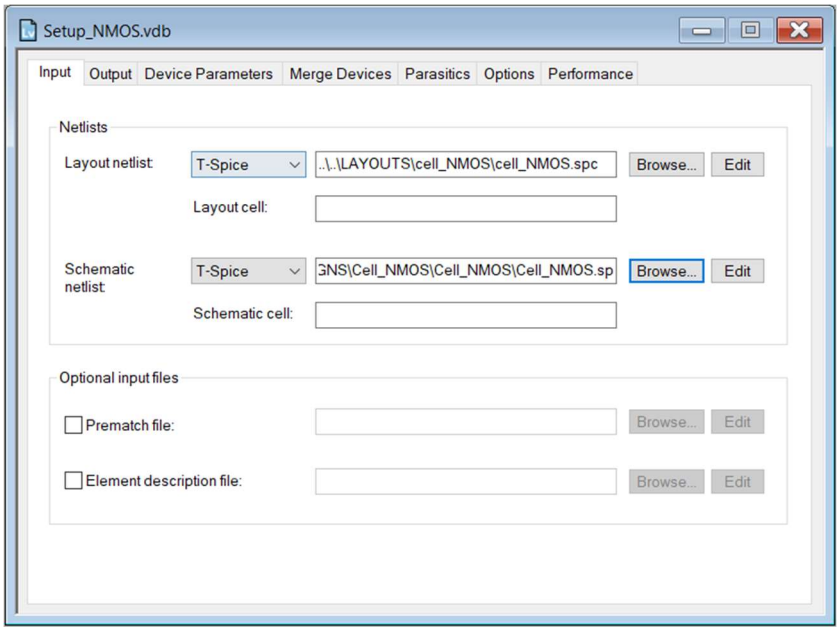


Figure 4: Setup of schematic and layout netlists.

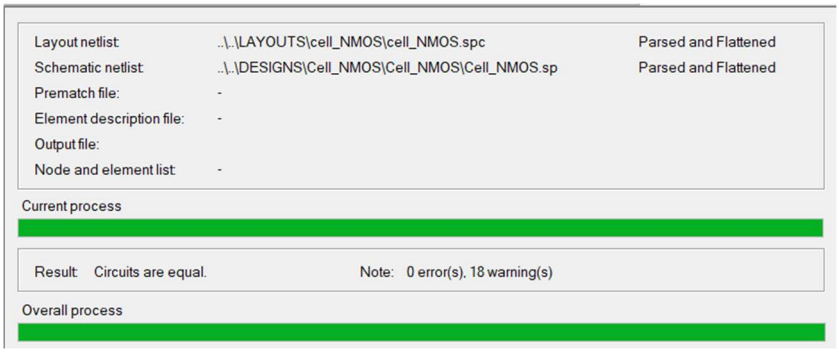


Figure 5: Verification results.

1.1.4 IDS-VDS Characteristics

Using the following SPICE command we generate the characteristic of drain current vs drain-source voltage for various values of gate-source voltages (Fig. 6). Command plotting Ids-Vds: *.dc lin param VDS 0v 3.3v 0.01v sweep VGS 0v 3.3v 0.3v, .print dc i(M1,D).* Also on this plot we see the threshold voltage for a drain-source voltage equal to 3.3V. Command plotting Ids-Vgs: *.dc lin param VGS 0v 3.3v 0.001 .print dc i(M1,D).*

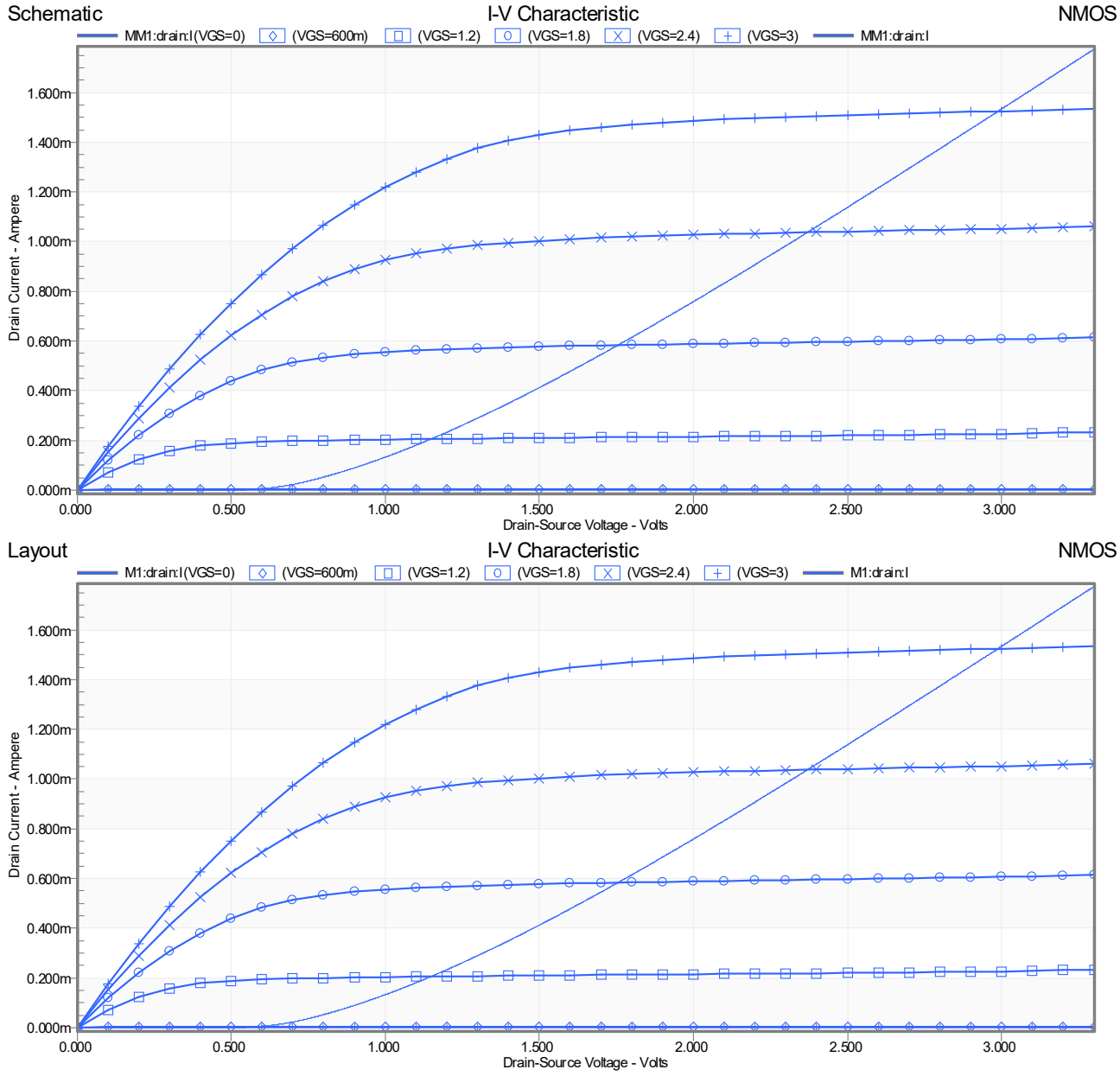


Figure 6: IDS-VDS characteristics schematic and layout design

From the simulation in (Fig. 6) we see the I-V characteristics. Studying these characteristics we distinguish three different regions of operation. The weak inversion where the gate voltage is lower than the threshold voltage (VGS<Vth). The linear region where drain-source voltage must be lower than overdrive voltage (VDS<VGS-Vth). The saturation region where drain-source voltage is equal or higher from the overdrive voltage (VDS≥VGS-Vth).

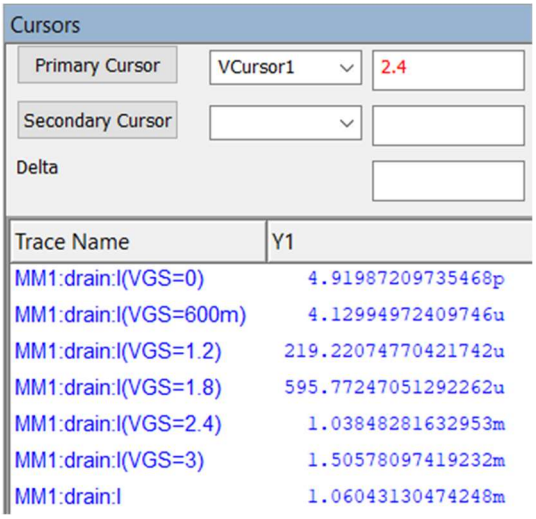


Figure 8: Schematic measurements VDS=2.4V.

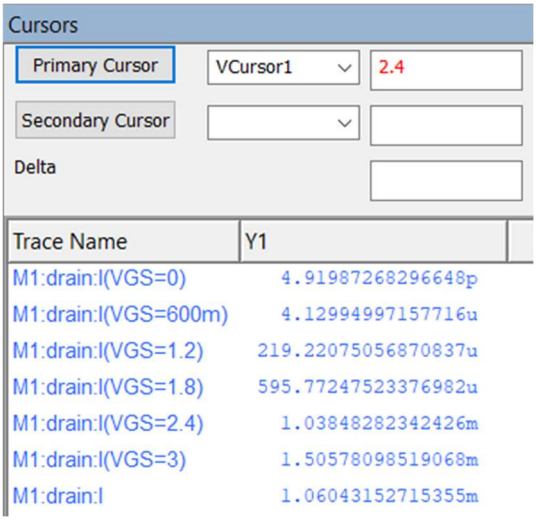


Figure 7: Layout measurements VDS=2.4V.

Figure 7 and (Fig. 8) show the drain current between the schematic and layout when VDS=2.4V. The currents are quite the same, any mismatch may occur because of the parasitic effects on the layout design.

1.1.5 IDS-VGS characteristic

Using the following SPICE command we generate the characteristics of threshold voltage for various values of drain-source voltages. Command plotting Ids-Vgs: *.dc lin param VGS 0v 3.3v 0.01v sweep VDS 0v 3.3v 0.6v, .print dc i(M1,D).*

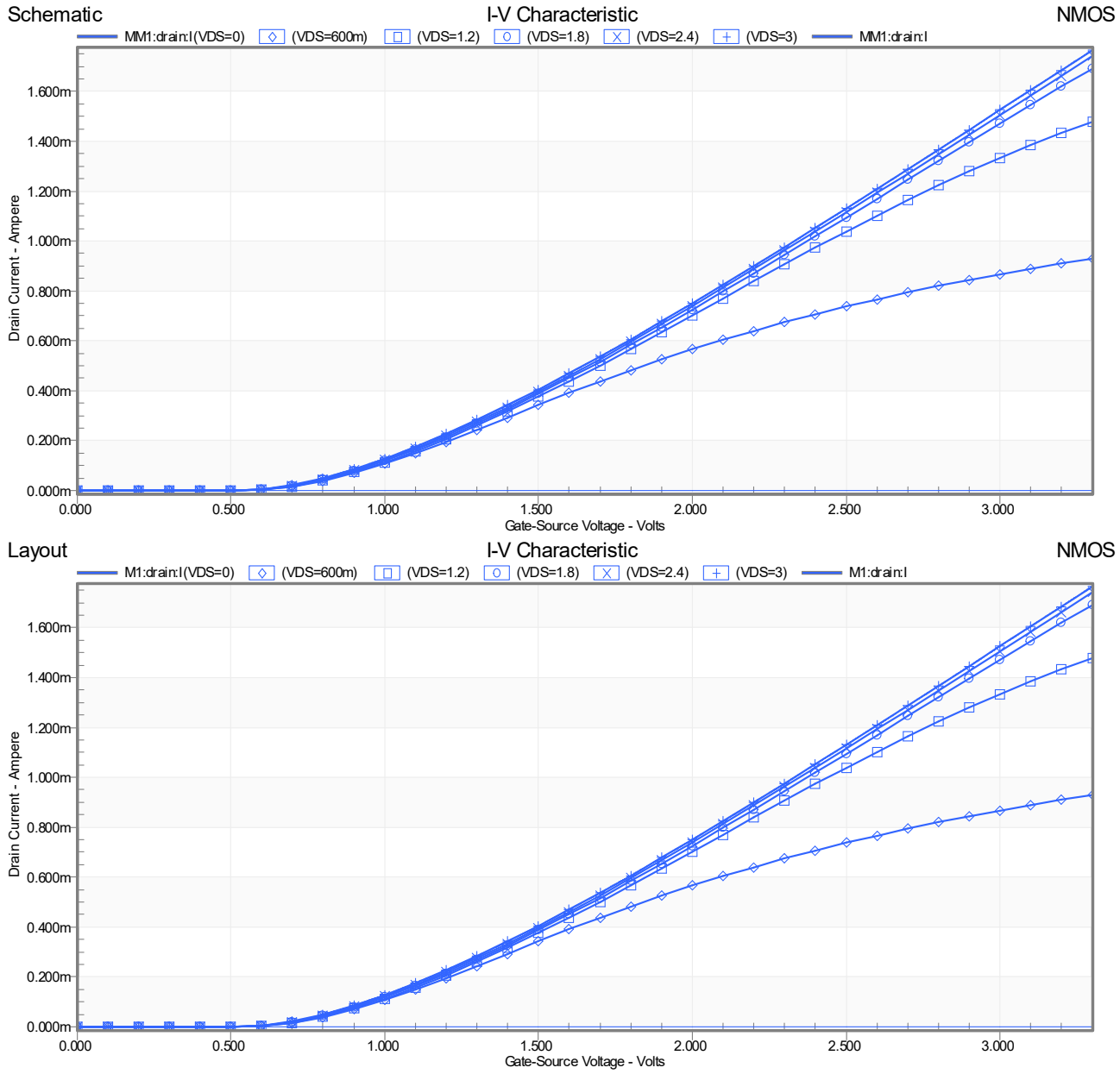


Figure 9: IDS-VGS schematic and layout design characteristic.

From simulation (Fig. 9) we can see that for different drain-source voltages we have different behavior of the threshold voltage. These different characteristics affect the three regions we discussed before.

1.1.6 Transconductance characteristic

Using the following SPICE command we generate the characteristic of transconductance for various values of gate-source voltages using drain-source voltage equal to 3.3V (Fig 10). Command plotting D(Ids)-Vgs*: .dc lin param VGS 0v 3.3v 0.001, .print dc gm(M1).*

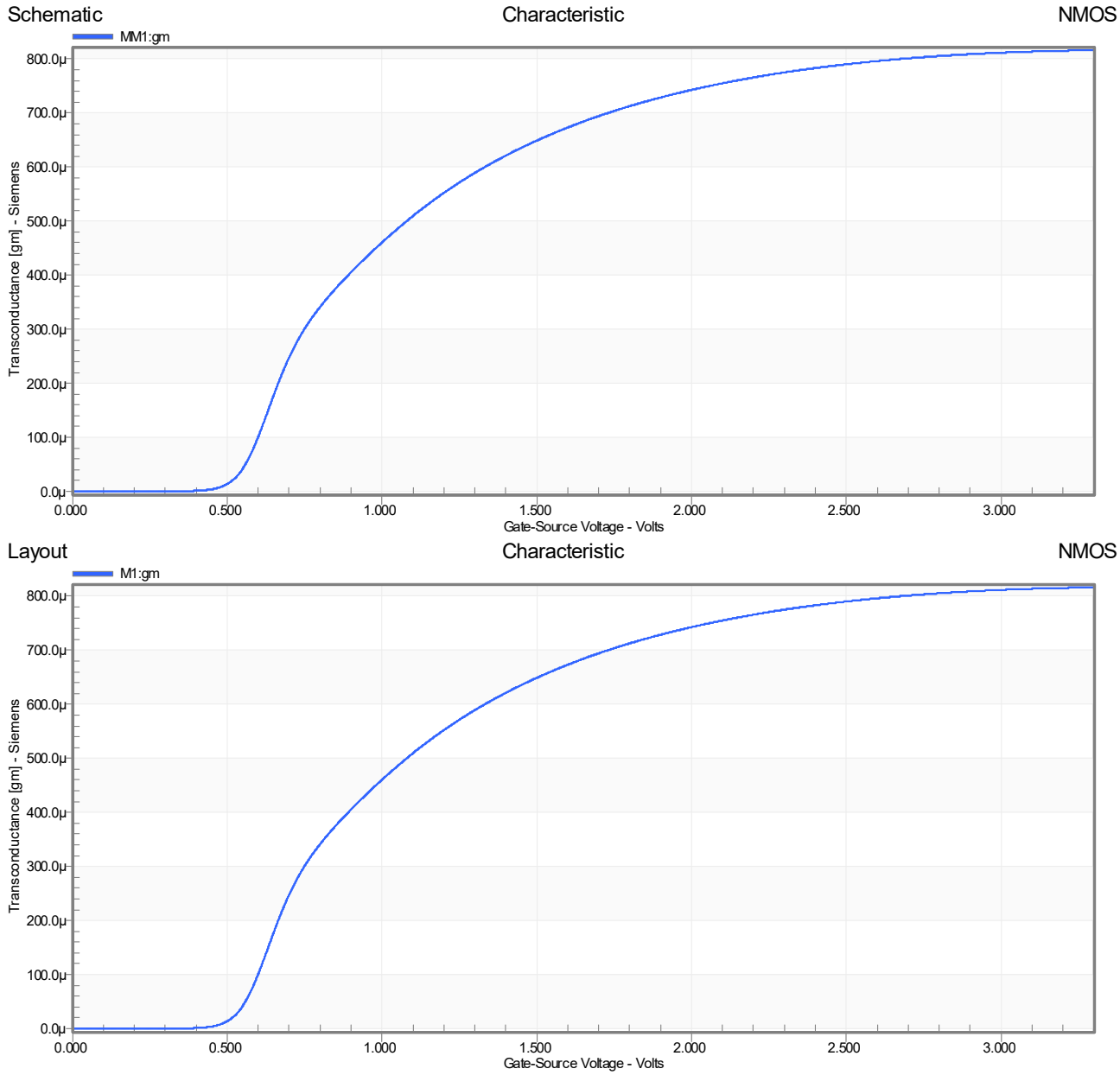


Figure 10: Transconductance characteristics of schematic and layout design.

Figure 10 shows the characteristic of transconductance. We can see clearly that increasing the gate-source voltage has as a result the increase of transconductance.

1.2 PMOS transistor structure

The PMOS (P-type Metal Oxide Semiconductor) transistor can be fabricated on a P-type substrate using an N-well layer. The device consists of two heavily-doped regions implanted with P-type material. This results in the forming of two regions also called as source and drain. Gate is a heavily-doped and conductive material consisting of a polysilicon layer. All the useful action of the device happens between the two terminals and the gate.

1.2.1 Schematic Design

On S-edit we setup the dc voltages VSG and VSD as parameters in the program. Using PMOS transistor with aspect ratio 10 and technology 0.35μm (Fig. 11). We use the SPICE model described on SPICE files section 5.2.

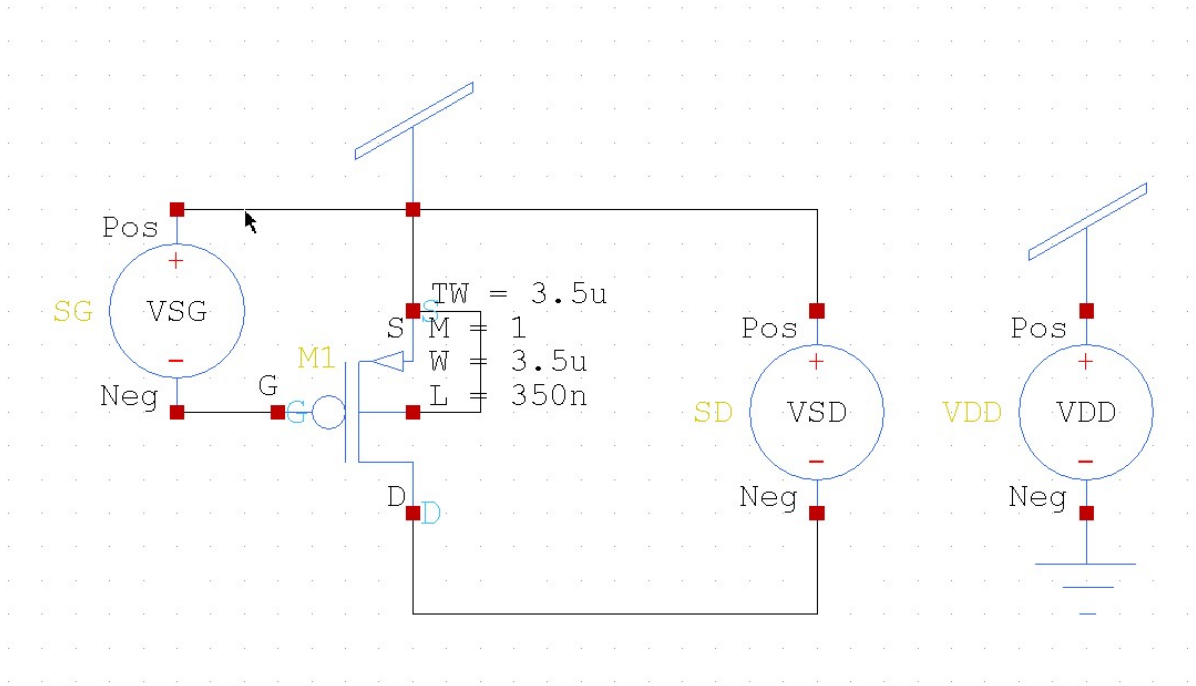


Figure 11: PMOS schematic design.

1.2.2 Layout Design

Using L-edit PMOS is fabricated on the substrate with N_Well layer and P_Implant layer for the drain and source. On top of P_Implant a layer called Active defines the area of the transistor called width (W). The gate of the transistor made with Poly layer and the bulk consists of N_impant with active on top. Contacts sit on top of a metal1 layer to achieve the connections between layers. Figure 12 shows the layout structure of the PMOS transistor. Figure 13 shows the cross section of the PMOS transistor.

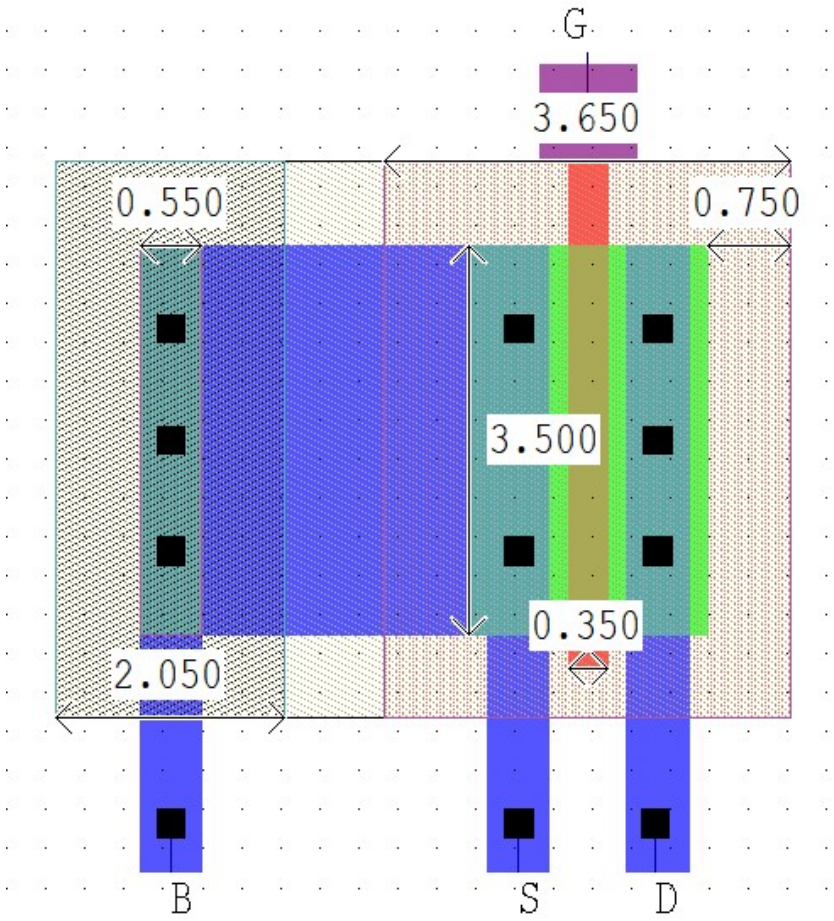


Figure 12: PMOS layout design.

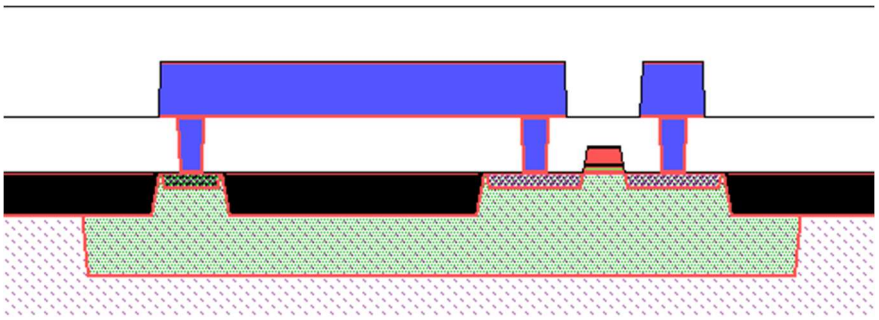


Figure 13: Cross-section of PMOS transistor.

1.2.3 Verification Layout vs Schematic

After the fabrication of layout and the schematic design we use the extract tool in order to obtain the netlist for the transistors. We use the LVS (Layout vs Schematic) tool to compare the netlists of the schematic (Netlist 3) and layout (Netlist 4) and verify that are equal (Fig. 14 and 15).

```
********************************************************************************
 * SPICE export by:  S-Edit 2019.2.0
 * Export time:     Wed Mar 29 11:50:52 2023
 * Design path:     C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\lib.defs
 * Library:         DESIGNS
 * Cell:           Cell_NMOS
 * Testbench:       Spice
 * View:           schematic
 * Export as:       top-level cell
 * Export mode:     hierarchical
 * Exclude empty:   yes
 * Exclude .model:  no
 * Exclude .hdl:    no
 * Exclude .end:    no
 * Expand paths:    yes
 * Wrap lines:      no
 * Exclude simulator commands:  no
 * Exclude global pins:        no
 * Exclude instance locations:  no
 * Control property name(s):    SPICE
 ********* Simulation Settings - General Section *********
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
 ********* Simulation Settings - Parameters *********
.param VSG = 3.3
.param VSD = 3.3
.param VDD = 3.3
***** Top Level *****
MM1 D G Vdd Vdd MODP W=3.5u L=350n AS=3.15p PS=8.8u AD=3.15p PD=8.8u $ $x=4500 $y=4500 $w=400
$h=600
VSD Vdd D  DC VSD $ $x=5900 $y=4500 $w=400 $h=600
VSG Vdd G  DC VSG $ $x=4000 $y=4800 $w=400 $h=600
VVDD Vdd Gnd  DC VDD $ $x=6700 $y=4500 $w=400 $h=600
.PLOT    I(MM1,D) $ $x=3700 $y=3700 $w=2000 $h=400 $r=180
.PLOT    gm(MM1) $ $x=12750 $y=4950 $w=3300 $h=300
 ********* Simulation Settings - Analysis Section *********
.op
.dc VSD 0v 3.3v 0.1 SWEEP VSG 0v 3.3v 0.6
 ********* Simulation Settings - Additional SPICE Commands *********
.dc lin param VSG 0v 3.3v 0.001
.end
```

Netlist 3: PMOS schematic netlist.

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Sun Mar 12 13:26:27 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_PMOS
* Write Flat:               NO
********************************************************************************
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
.temp 25
**************************************
.param VSD=3.3
.param VSG=3.3
.param VDD=3.3
**************************************
M1 D G VDD VDD MODP l=3.5e-07 w=3.5e-06 ad=3.15e-12 as=3.15e-12 pd=8.8e-06 ps=8.8e-06  $ (35.84
13.123 36.19 16.623)
**************************************
VSD VDD D  DC VSD
VSG VDD G VSG DC VSG
VSD1 VDD GND DC VDD
**************************************
.dc lin param VSD 0v 3.3v 0.1 sweep lin param VSG 0v 3.3v 0.6
.dc lin param VSG 0v 3.3v 0.001
**************************************
.print dc i(M1,D)
.print dc gm(M1)
**************************************
* Top level device count
* M(PMOS25)                  1
* Number of devices:         1
* Number of nodes:  3
```

Netlist 4: PMOS layout netlist.

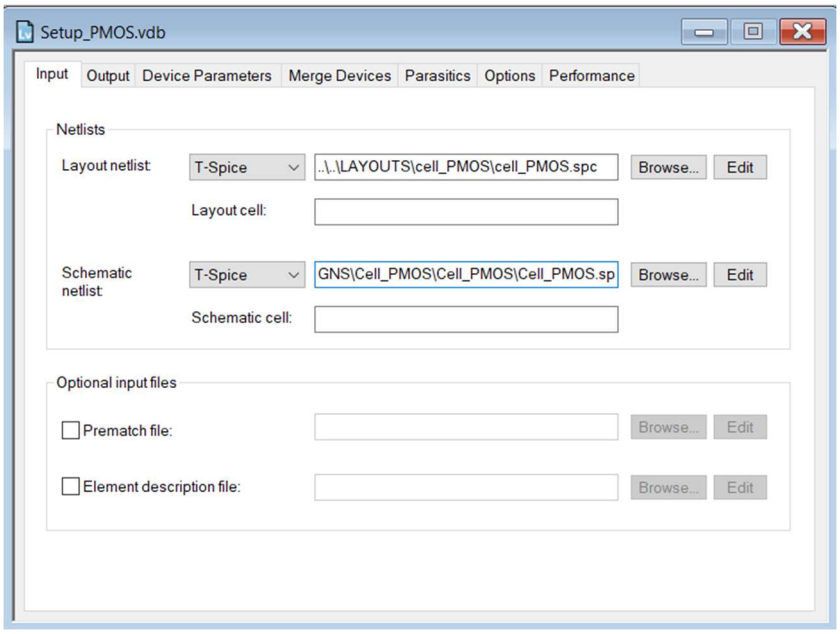


Figure 14: Setup of schematic and layout netlists.

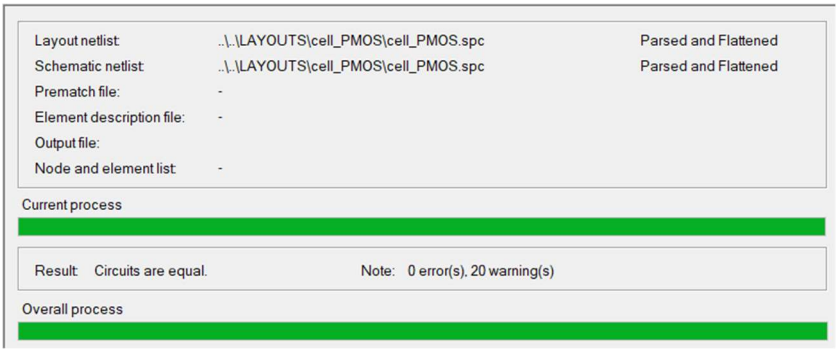


Figure 15: Verification results.

1.2.4 IDS-VDS Characteristics

Using the following SPICE command we generate the characteristic of drain current vs source-drain voltage for various values of source-gate voltages (Fig 16). Command plotting Ids-Vsd: *.dc lin param VSD 0v 3.3v 0.01v sweep VSG 0v 3.3v 0.3v, .print dc i(M1,D).* Also on this plot we see the threshold voltage for source-drain voltage equal to 3.3V. Command plotting Ids-Vsg: *.dc lin param VSG 0v 3.3v 0.001, .print dc i(M1,D).*

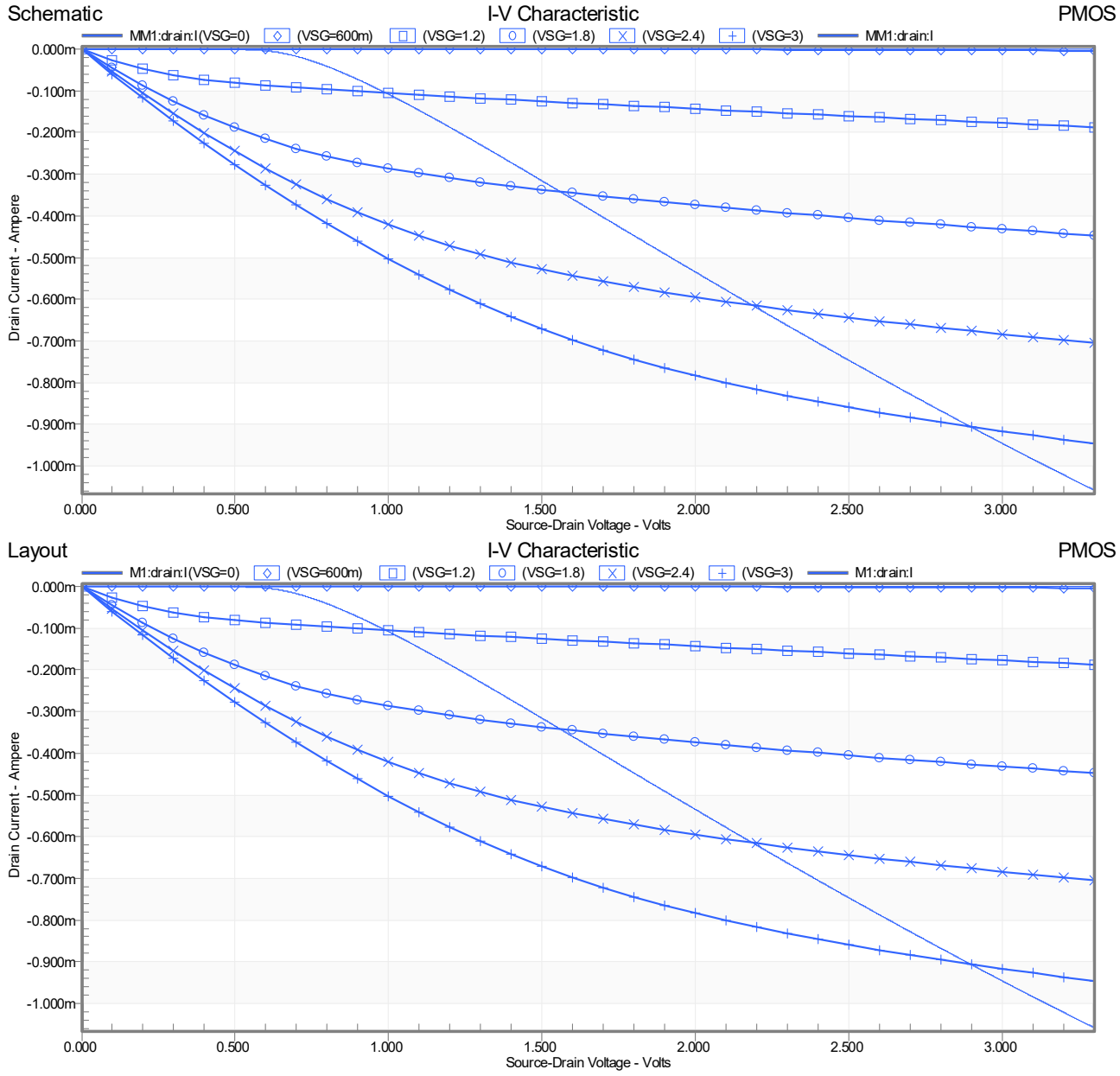


Figure 16: IDS-VGS characteristics schematic and layout design

From the simulation in (Fig. 16) we see the I-V characteristics. Studying these characteristics we distinguish three different regions of operation. The weak inversion where the gate voltage is lower than the threshold voltage (VSG<|Vth|). The linear region where source-drain voltage must be lower than overdrive voltage (VSD<VSG-|Vth|). The saturation region where source-drain voltage is equal or higher from the overdrive voltage (VSD≥-VSG-|Vth|).

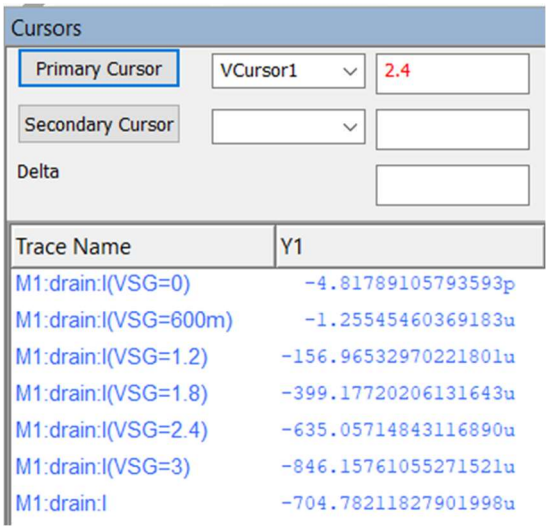


Figure 18: Schematic measurements VSD=2.4V

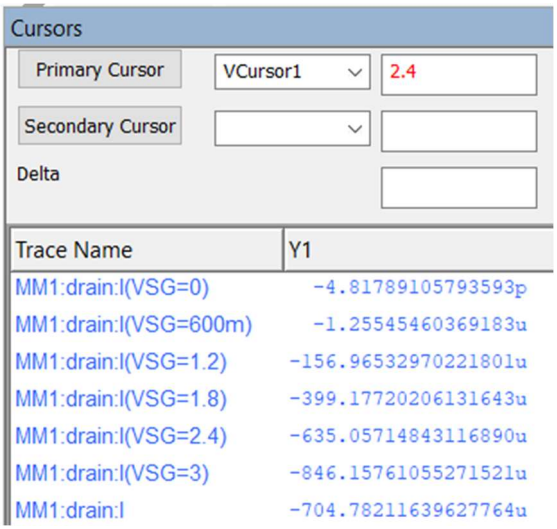


Figure 17: Layout measurements VSD=2.4V

Figure 17 and (Fig. 18) show the drain current between the schematic and layout when VSD=2.4V. The currents are quite the same, any mismatch may occur because of the parasitic effects on the layout design.

1.2.5 IDS-VGS characteristic of PMOS

Using the following SPICE command we generate the characteristics of threshold voltage for various values of source-drain voltages. Command plotting Ids-Vsg: *.dc lin param VSG 0v 3.3v 0.01v sweep VSD 0v 3.3v 0.6v, .print dc i(M1,D).*

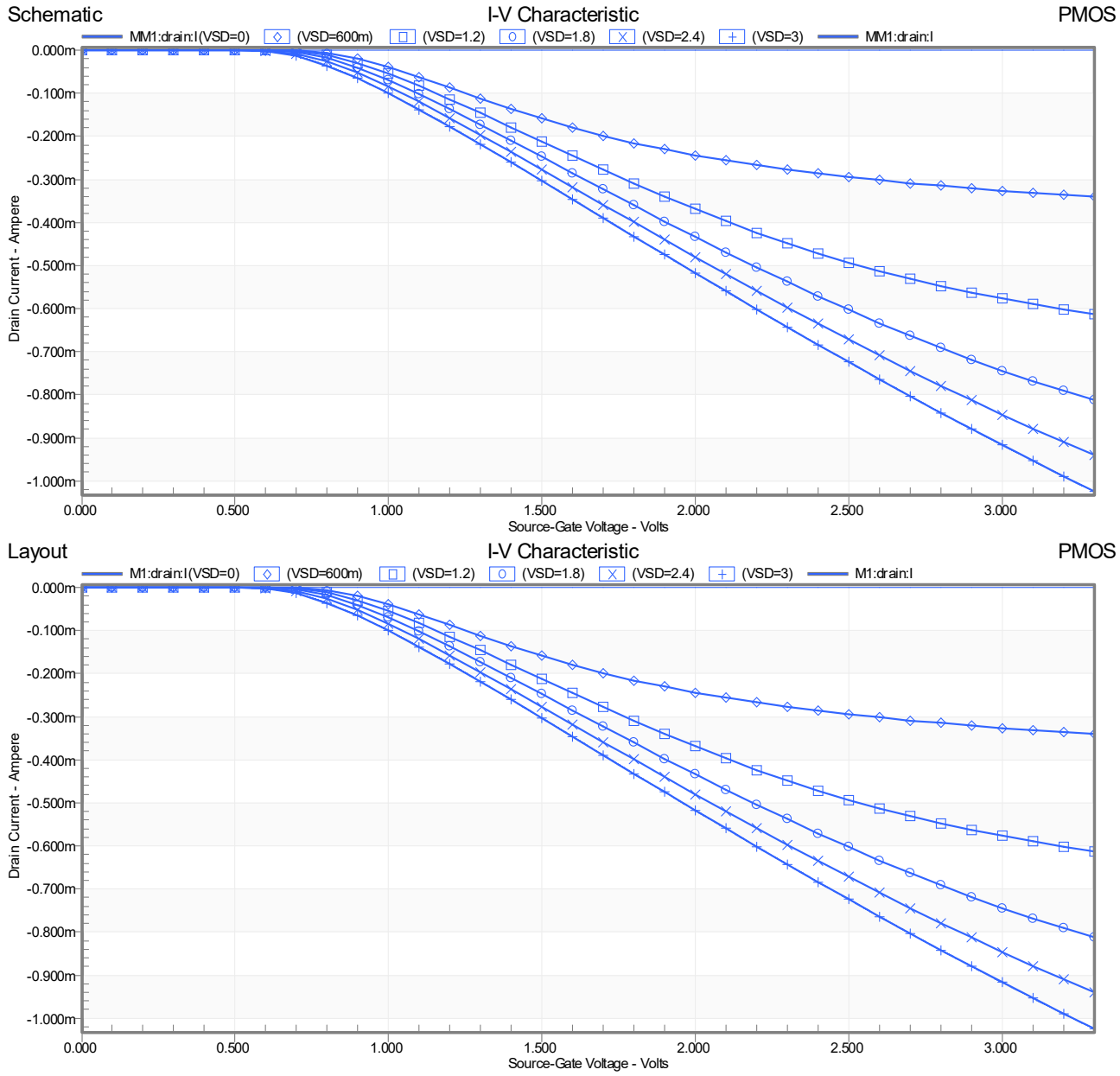


Figure 19: IDS-VSG characteristics for schematic and layout design.

From simulation in (Fig. 19) we can see that for different source-drain voltages we have different behaviour of the threshold voltages. These different characteristics affect the three regions we discussed before.

1.2.6 Transconductance characteristic

Using the following SPICE command we generate the characteristic of transconductance for various values of source-gate voltages using source-drain voltage equal to 3.3V (Fig 20). Command plotting D(Ids)-Vsg: *.dc lin param VSG 0v 3.3v 0.001, .print dc gm(M1).*

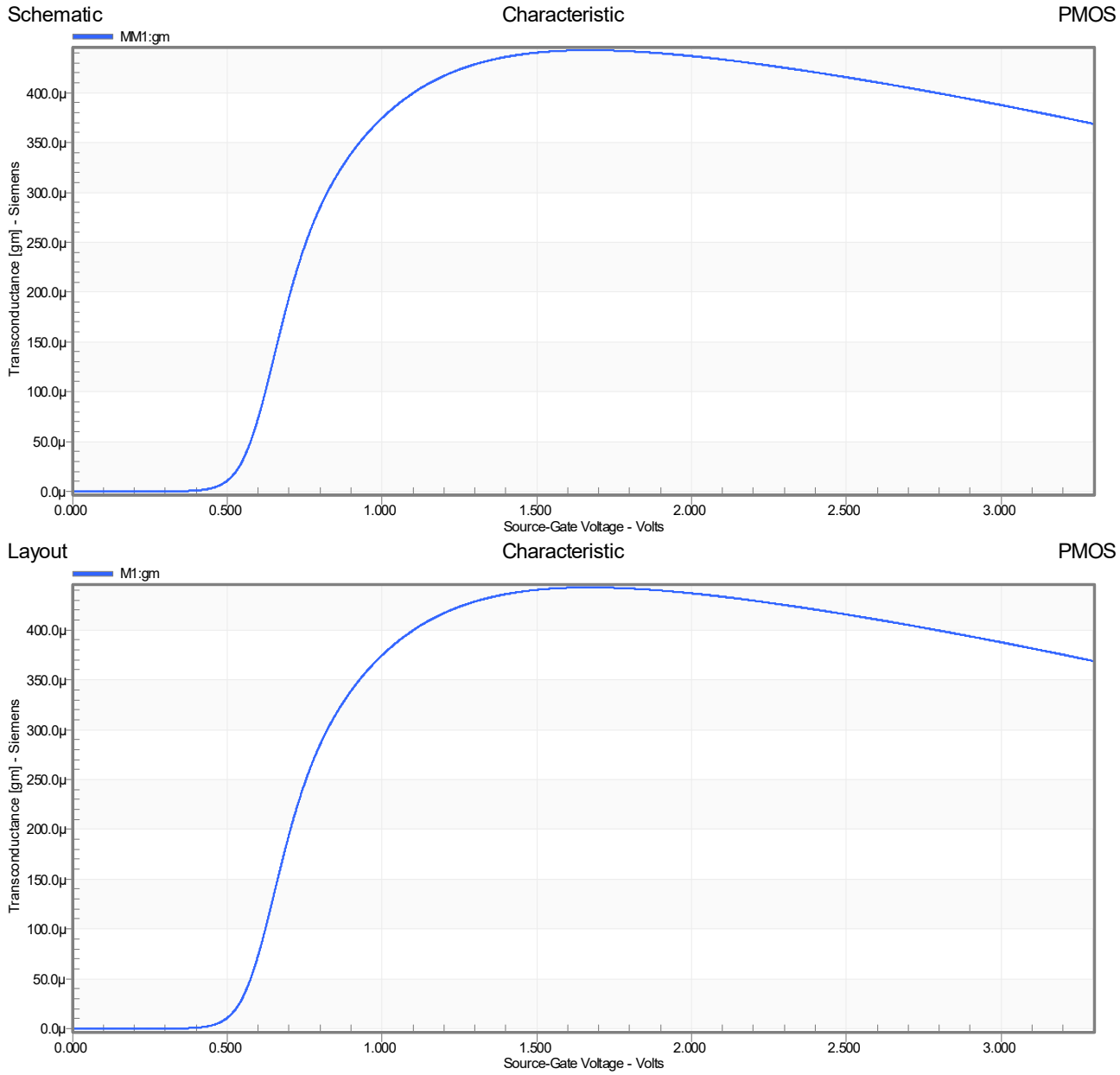


Figure 20: Transconductance characteristics for schematic and layout design.

Figure 20 shows the characteristic of transconductance. We can see clearly that increasing the source-gate voltage has as a result the increase of transconductance.

1.3 Diode connected transistors

Using the diode connected configuration we achieve a two terminal device. This configuration works if we connect gate and drain terminals of the device. The idea behind this configuration is that the transistor always operates in the saturation region. Figure 21 shows the different sizing of NMOS and PMOS transistors using diode connection configuration. Figure 22 shows the layout design based on schematic of (Fig. 21).

1.3.1 Schematic design of CMOS diode connected transistors

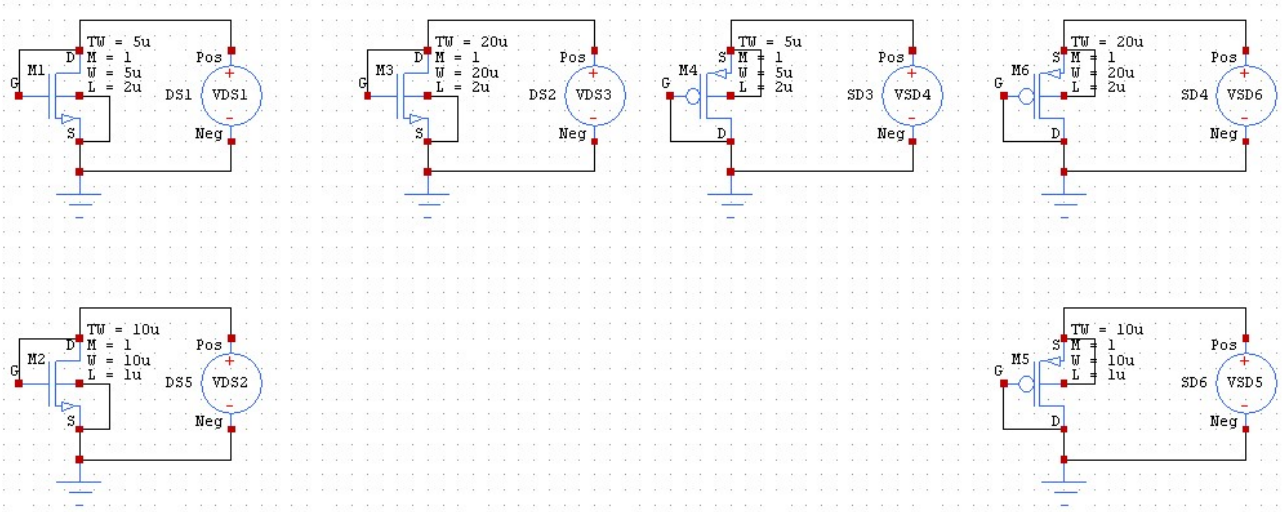


Figure 21: Schematic design of CMOS diode connected transistors.

1.3.2 Layout design of diode connected transistors

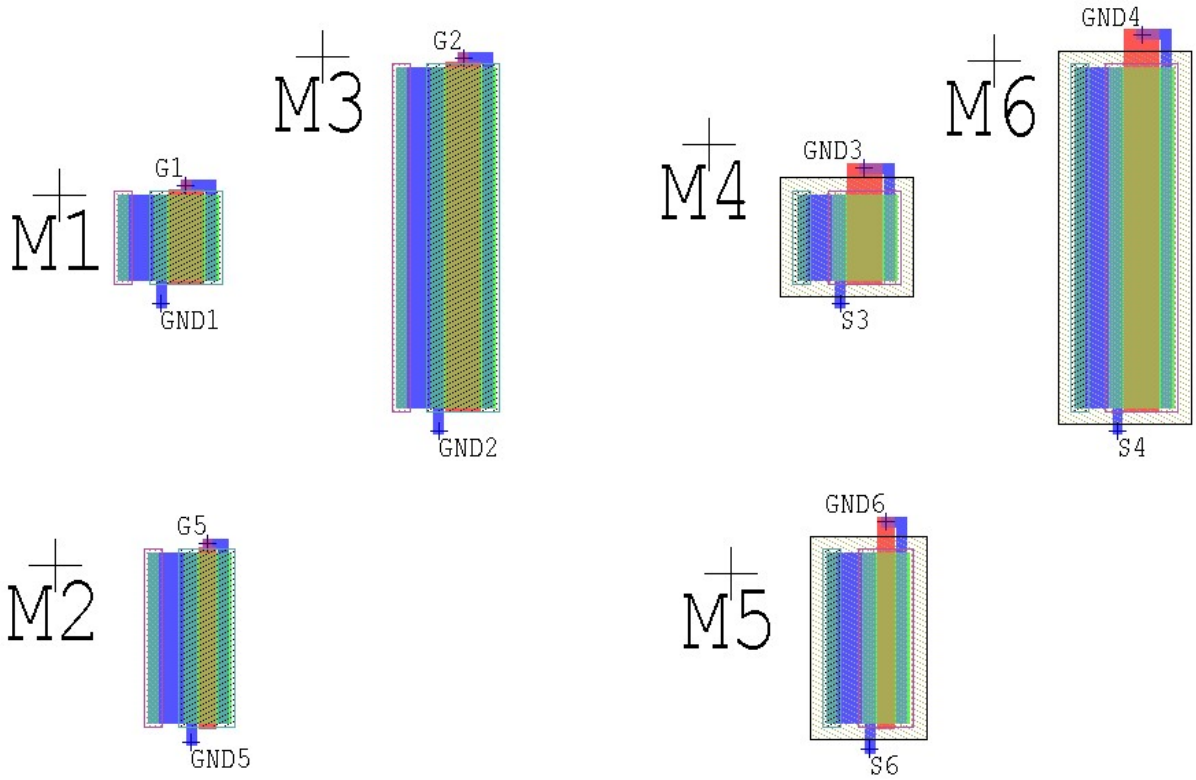


Figure 22: Layout design of diode connected transistors.

1.3.3 Netlist of diode connected transistors

After the fabrication of layout and schematic design we use the extract tool in order to obtain the netlist for the transistors. We use the LVS (Layout vs Schematic) tool to compare the netlists of the schematic (Netlist 5) and layout (Netlist 6) and verify that are equal (Fig. 23).

```
**********************************************************************
* SPICE export by:  S-Edit 2019.2.0
* Export time:      Fri May 12 11:37:04 2023
* Design path:      C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\lib.defs
* Library:          DESIGNS
* Cell:             Cell_DIODE_CMOS
* Testbench:        Spice
* View:             schematic
* Export as:        top-level cell
* Export mode:      hierarchical
* Exclude empty:    yes
* Exclude .model:   no
* Exclude .hdl:     no
* Exclude .end:     no
* Expand paths:     yes
* Wrap lines:       no
* Exclude simulator commands:  no
* Exclude global pins:         no
* Exclude instance locations:  no
* Control property name(s):    SPICE
********* Simulation Settings - General Section *********
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\SPICE_MODELS\LEVEL1\SPICELEVEL1_Tech_0.5um.lib"
********* Simulation Settings - Parameters *********
.param VDS2 = 1.2V
.param VSD3 = 1.2V
.param VSD4 = 1.2V
.param VDS5 = 1.2V
.param VSD6 = 1.2V
.param VDS1 = 1.2V
***** Top Level *****
MM1 N_1 N_1 Gnd Gnd MODN W=5u L=2u AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=1200
$y=3700 $w=400 $h=600
MM2 N_3 N_3 Gnd Gnd MODN W=10u L=1u AS=9p PS=21.8u AD=9p PD=21.8u $ $x=1200 $y=1800
$w=400 $h=600
MM3 N_2 N_2 Gnd Gnd MODN W=20u L=2u AS=18p PS=41.8u AD=18p PD=41.8u $ $x=3500
$y=3700 $w=400 $h=600
MM4 Gnd Gnd N_4 N_4 MODP W=5u L=2u AS=4.5p PS=11.8u AD=4.5p PD=11.8u $ $x=5500 $y=3700
$w=400 $h=600
MM5 Gnd Gnd N_6 N_6 MODP W=10u L=1u AS=9p PS=21.8u AD=9p PD=21.8u $ $x=7700 $y=1800
$w=400 $h=600
MM6 Gnd Gnd N_5 N_5 MODP W=20u L=2u AS=18p PS=41.8u AD=18p PD=41.8u $ $x=7700 $y=3700
$w=400 $h=600
VDS1 N_1 Gnd  DC VDS1 $ $x=2400 $y=3700 $w=400 $h=600
VDS2 N_2 Gnd  DC VDS3 $ $x=4800 $y=3700 $w=400 $h=600
VDS5 N_3 Gnd  DC VDS2 $ $x=2400 $y=1800 $w=400 $h=600
VSD3 N_4 Gnd  DC VSD4 $ $x=6900 $y=3700 $w=400 $h=600
VSD4 N_5 Gnd  DC VSD6 $ $x=9100 $y=3700 $w=400 $h=600
```

```
VSD6 N_6 Gnd  DC VSD5 $ $x=9100 $y=1800 $w=400 $h=600
********* Simulation Settings - Analysis Section *********
.op
********* Simulation Settings - Additional SPICE Commands *********
.end
```

Netlist 5: Schematic of diode connected transistors.

```
*******************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Mon Mar 13 11:46:38 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_DIODE_CONNECTED_CMOS
* Write Flat:               NO
*******************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\SPICE_MODELS\LEVEL1\SPICELEVEL1_Tech_0.5um.lib"
********* Simulation Settings - Parameters *********
.param VDS1 = 1.2V
.param VDS2 = 1.2V
.param VDS3 = 1.2V
.param VSD4 = 1.2V
.param VSD5 = 1.2V
.param VSD6 = 1.2V
**************************************
M1 G1 G1 GND1 GND1 MODN l=2e-06 w=5e-06 ad=4.5e-12 as=4.5e-12 pd=1.18e-05 ps=1.18e-05  $ (31.97
21.943 33.97 26.943)
M2 G2 G2 GND2 GND2 MODN l=1e-06 w=1e-05 ad=9e-12 as=9e-12 pd=2.18e-05 ps=2.18e-05  $ (33.73 -4.16
34.73 5.84)
M3 G3 G3 GND3 GND3 MODN l=2e-06 w=2e-05 ad=1.8e-11 as=1.8e-11 pd=4.18e-05 ps=4.18e-05  $ (48.32
14.443 50.32 34.443)
M4 GND4 GND4 S4 S4 MODP l=2e-06 w=5e-06 ad=4.5e-12 as=4.5e-12 pd=1.18e-05 ps=1.18e-05  $ (71.97
21.943 73.97 26.943)
M5 GND5 GND5 S5 S5 MODP l=1e-06 w=1e-05 ad=9e-12 as=9e-12 pd=2.18e-05 ps=2.18e-05  $ (73.73 -4.16
74.73 5.84)
M6 GND6 GND6 S6 S6 MODP l=2e-06 w=2e-05 ad=1.8e-11 as=1.8e-11 pd=4.18e-05 ps=4.18e-05  $ (88.32
14.443 90.32 34.443)
**************************************
VDS1 G1 GND1 DC VDS1
VDS2 G2 GND2 DC VDS2
VDS3 G3 GND3 DC VDS3
VSD4 S4 GND4 DC VSD4
VSD5 S5 GND5 DC VSD5
VSD6 S6 GND6 DC VSD6
**************************************
.op
**************************************
* Top level device count
* M(NMOS25)                  3
* M(PMOS25)                  3
```

```
* Number of devices:      6
* Number of nodes:  11
```

Netlist 6: Layout netlist of diode transistors.

1.3.4 Verification of Layout vs Schematic for diode connected transistors

The importance of LVS (Layout vs Schematic) is to determine if the devices that are designed using the physical tool have the same connections and pins with schematic.

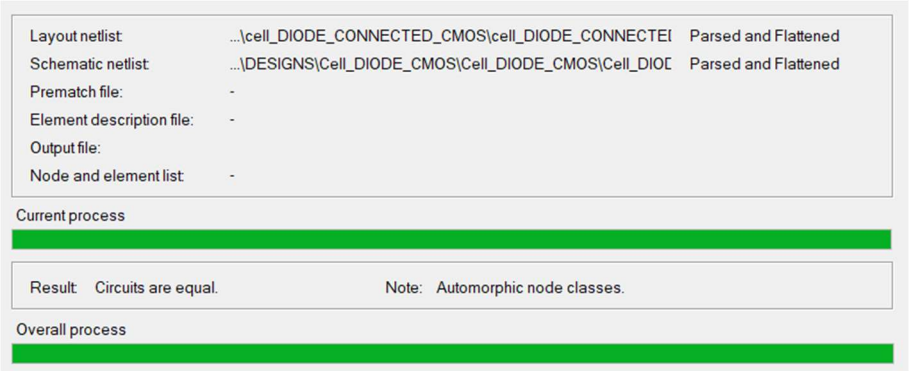


Figure 23: Verification results.

1.3.5 SPICE simulation results of CMOS diode connected transistors

AC SMALL-SIGNAL MODELS: temperature=25.0

	0	1	2	3
	M1	M2	M3	M4
MODEL	MODN	MODN	MODN	MODP
TYPE	NMOS	NMOS	NMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	51.0880u	223.8142u	204.3521u	-10.4564u
IBS	0.	0.	0.	0.
IBD	-54.0000e-021	-108.0000e-021	-216.0000e-021	27.0000e-021
VGS	1.2000	1.2000	1.2000	-1.2000
VDS	1.2000	1.2000	1.2000	-1.2000
VBS	0.	0.	0.	0.
VTH	700.0000m	700.0000m	700.0000m	-800.0000m
VDSAT	500.0000m	500.0000m	500.0000m	-400.0000m
BETA	364.9144u	1.5987m	1.4597m	105.4070u
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	204.6989u	896.7760u	818.7955u	52.3928u
GDS	4.5614u	19.9834u	18.2457u	1.6865u
GMB	47.5278u	208.2170u	190.1112u	11.3900u
GBD	45.0000e-021	90.0000e-021	180.0000e-021	22.5000e-021
GBS	45.0000e-021	90.0000e-021	180.0000e-021	22.5000e-021
CDTOT	15.5219f	18.2491f	62.0716f	15.9362f
CGTOT	38.8334f	39.2987f	155.3337f	38.1416f
CSTOT	15.8612f	18.9267f	63.4258f	17.6307f
CBTOT	16.0821f	19.3632f	64.2936f	18.7020f
CGS	13.3010f	13.8125f	53.2038f	13.3649f
CGD	13.7662f	14.7431f	55.0649f	13.1383f
CGB	11.7662f	10.7431f	47.0649f	11.6383f
CBD	1.7560f	3.5066f	7.0080f	2.7985f
CBS	2.5613f	5.1163f	10.2263f	4.2678f

	4	5
	M5	M6
MODEL	MODP	MODP
TYPE	PMOS	PMOS
REGION	Saturation	Saturation
ID	-46.4161u	-41.8255u
IBS	0.	0.
IBD	54.0000e-021	108.0000e-021
VGS	-1.2000	-1.2000
VDS	-1.2000	-1.2000
VBS	0.	0.
VTH	-800.0000m	-800.0000m
VDSAT	-400.0000m	-400.0000m
BETA	467.9042u	421.6280u
RS	0.	0.
RD	0.	0.
GM	232.5728u	209.5711u
GDS	7.4865u	6.7460u
GMB	50.5605u	45.5600u
GBD	45.0000e-021	90.0000e-021
GBS	45.0000e-021	90.0000e-021
CDTOT	19.0786f	63.7316f
CGTOT	37.9150f	152.5663f
CSTOT	22.4662f	70.5054f
CBTOT	24.6044f	74.7773f
CGS	13.9404f	53.4596f
CGD	13.4873f	52.5534f
CGB	10.4873f	46.5534f
CBD	5.5925f	11.1805f
CBS	8.5298f	17.0538f

Figure 24: SPICE results of diode connected CMOS transistors.

The SPICE calculations provide some important information about the device behavior. Considering the device M3 and M6 (Fig. 24) and by looking the sizing of transistors it is expected that the drain current (ID) should be four times the current of M1 and M4. From the transconductance and output conductance equation because the current is four times larger we can expect that the transconductances (gm) and output conductances (gds) should be also four times larger. Looking the devices M2 and M5 it is obvious that have the same aspect ratio with the devices M3 and M6 but they don't achieve the same results. For example we see that the current of M2 and M5 is 10% larger from M3 and M6 (Fig. 24). That is because we have different shortening of the channel length for the devices.

1.3.6 MATLAB calculations for M1 NMOS diode connected transistor

Calculations with MATLAB for transistor M1 (W/L)=2.5 the process transconductance parameter (kn), transconductance (gm) and the output conductance (gds) based on CMOS equations using level 1 SPICE model for 0.5μm. SPICE files section 5.1.

$$C_{ox} = \frac{\varepsilon_0 \cdot \varepsilon_{r,ox}}{t_{ox}} \quad (1)$$

$$k_n = \mu_n \cdot C_{ox} \quad (2)$$

$$k_p = \mu_p \cdot C_{ox} \quad (3)$$

$$I_D = \frac{1}{2} k_n \frac{W}{L} \left(V_{gs} - V_{th}\right)^2 (1 + \lambda V_{ds}) \quad (4)$$

$$g_m = \frac{2I_D}{V_{gs} - V_{th}} \quad (5)$$

$$g_{ds} = \lambda \cdot I_D \quad (6)$$

With code 1 we calculate the process transconductance based on eq. 2 which is important parameter to calculate the current of the device. Before the calculation of transconductance it is important to define the value of oxide capacitance based on eq. 1.

```
%process transconductance parameter for n-channel
tox=9*10^-9;                    %[m] spice referenced as TOX in [nm]
mn=350*10^-4;                   %[m^2/V-sec] spice referenced as UO in [cm^2/V-sec]
e0=8.858*10^-14*10^2;           %[F/m]
er_ox=3.9;                      %[]

Cox_result=Cox_function(e0,er_ox,tox);
kn_result=kn_function(mn,Cox_result);
fprintf('oxide capacitance: Cox=%d [F/m^2]\n',Cox_result);
fprintf('transconductance parameter for n-channel: kn=%d [A/V^2]\n',kn_result);

function kn_result=kn_function(mn,Cox)
kn_result=mn*Cox;
end

function Cox_result=Cox_function(e0,er_ox,tox)
Cox_result=(e0*er_ox)/tox;
end
```

```
                    oxide capacitance: Cox=3.838467e-03 [F/m^2]
          transconductance parameter for n-channel: kn=1.343463e-04 [A/V^2]
```

Code 1: MATLAB calculation for M1 transistor process transconductance parameter.

With code 2 we calculate the drain current using eq. 4.

```
%Calculation of ID n-channel in saturation region
Vth=700.0000*10^-3;     %[V]
Vgs=1.2;                %[V]
Vds=1.2;                %[V]
kn=1.343463*10^-4;      %[A/V^2]
L=2*10^-6;              %[m]
W=5*10^-6;              %[m]
lambda=0.1;             %[1/m]

Idnsaturation_result=Idnsaturation_function(kn,Vgs,Vth,W,L,lambda,Vds);
fprintf('ID n-channel in saturation region: Id=%d [A]\n',Idnsaturation_result);

function Idnsaturation_result=Idnsaturation_function(kn,Vgs,Vth,W,L,lambda,Vds)
Idnsaturation_result=(1/2)*kn*(W/L)*((Vgs-Vth)^2)*(1+lambda*Vds);
end
```

```
                ID n-channel in saturation region: Id=4.702120e-05 [A]
```

Code 2: MATLAB calculation for M1 transistor saturation current.

With code 3 we calculate the transconductance parameter using eq. 5.

```
%transconductance gm saturation region n-channel
Idsat=4.702120e-05;  %[A]
Vgs=1.2;                %[V]
Vth=700.0000*10^-3;     %[V]
gmsaturationn1_result=gmsaturationNtype1_function(Idsat,Vgs,Vth);
fprintf('transconductance saturation region n-channel: gm=%d
[A/V]\n',gmsaturationn1_result);

function gmsaturationn1_result=gmsaturationNtype1_function(Idsat,Vgs,Vth)
gmsaturationn1_result=(2*Idsat)/(Vgs-Vth);
end
```

```
          transconductance saturation region n-channel: gm=1.880848e-04 [A/V]
```

Code 3: MATLAB calculation for M1 transistor transconductance parameter.

With code 4 we calculate the output conductance parameter using eq. 6.

```
%calculation of output conductance gds n-channel saturation region
Idnsat=4.702120e-05;  %[A]
lambda=0.1;           %[1/m]
gdssaturationn_result=gdssaturationNtype_function(lambda,Idnsat);
fprintf('output conductance n-channel saturation region: gds=%d
[A/V]\n',gdssaturationn_result);

function gdssaturationn_result=gdssaturationNtype_function(lambda,Idnsat)
gdssaturationn_result=lambda*Idnsat;
end
```

```
output conductance n-channel saturation region: gds=4.702120e-06 [A/V]
```

Code 4: MATLAB calculation for M1 transistor output conductance parameter.

1.3.7 MATLAB calculations for M4 PMOS diode connected transistor

Calculations with MATLAB for transistor M4 (W/L)=2.5 the process transconductance parameter (kp), transconductance (gm) and the output conductance (gds) based on CMOS equations using level 1 SPICE model for 0.5μm. SPICE files section 5.1.

With code 5 we calculate the process transconductance based on eq. 2 which is important parameter to calculate the current of the device. Before the calculation of transconductance it is important to define the value of oxide capacitance based on eq. 1.

```
%process transconductance parameter for p-channel
tox=9*10^-9;                    %[m] spice referenced as TOX in [nm]
mp=100*10^-4;                   %[m^2/V-sec] spice referenced as UO in [cm^2/V-sec]
e0=8.858*10^-14*10^2;           %[F/m]
er_ox=3.9;                      %[]
Cox_result=Cox_function(e0,er_ox,tox);
kp_result=kp_function(mp,Cox_result);
fprintf('oxide capacitance: Cox=%d [F/m^2]\n',Cox_result);
fprintf('transconductance parameter for p-channel: kp=%d [A/V^2]\n',kp_result);

function kp_result=kp_function(mp,Cox)
kp_result=mp*Cox;
end

function Cox_result=Cox_function(e0,er_ox,tox)
Cox_result=(e0*er_ox)/tox;
end
```

```
                    oxide capacitance: Cox=3.838467e-03 [F/m^2]
          transconductance parameter for p-channel: kp=3.838467e-05 [A/V^2]
```

Code 5: MATLAB calculation for M4 transistor process transconductance parameter.

With code 2 we calculate the drain current using eq. 4.

```
%Calculation of ID p-channel in saturation region
Vth=-800.0000*10^-3;      %[V]
Vgs=-1.2;                 %[V]
Vds=-1.2;                 %[V]
L=2*10^-6;                %[m]
W=5*10^-6;                %[m]
kp=3.838467e-05;          %[A/V^2]
lambda=0.2;               %[1/m]

Idpsaturation_result=Idpsaturation_function(kp,W,L,Vgs,Vth,lambda,Vds);
fprintf('ID p-channel saturation region: Id=%d [A]\n',Idpsaturation_result);

function Idpsaturation_result=Idpsaturation_function(kp,W,L,Vgs,Vth,lambda,Vds)
Idpsaturation_result=(1/2)*kp*(W/L)*abs((Vgs-Vth)^2)*(1+lambda*abs(Vds));
end
```

```
                ID p-channel saturation region: Id=9.519398e-06 [A]
```

Code 6: MATLAB calculation for M4 transistor saturation current.

With code 7 we calculate the transconductance parameter using eq. 5.

```
%transconductance gm saturation region p-channel
Idsat=9.519398e-06;  %[A]
Vgs=-1.2;              %[V]
Vth=-800.0000*10^-3; %[V]
gmsaturationp1_result=gmsaturationPtype1_function(Idsat,Vgs,Vth);
fprintf('transconductance saturation region p-channel: gm=%d
[A/V]\n',gmsaturationp1_result);

function gmsaturationp1_result=gmsaturationPtype1_function(Idsat,Vgs,Vth)
gmsaturationp1_result=(2*Idsat)/(abs(Vgs-Vth));
end
```

```
transconductance saturation region p-channel: gm=4.759699e-05 [A/V]
```

Code 7: MATLAB calculation for M4 transistor transconductance parameter.

With code 8 we calculate the output conductance parameter eq.6.

```
%calculation of output conductance gds p-channel saturation region
Idpsat=9.519398e-06;  %[A]
lambda=0.2;           %[1/m]
gdssaturationp_result=gdssaturationPtype_function(lambda,Idpsat);
fprintf('output conductance p-channel saturation region gds=%d
[A/V]\n',gdssaturationp_result);

function gdssaturationp_result=gdssaturationPtype_function(lambda,Idpsat)
gdssaturationp_result=lambda*Idpsat;
end
```

```
output conductance p-channel saturation region gds=1.903880e-06 [A/V]
```

Code 8: MATLAB calculation for M4 transistor output conductance parameter.

Table 1 shows the calculated parameters using MATLAB and SPICE parameters extracted using simulation.

Parameters	Calculated	Spice
M1 I_D	47.702120u [A]	51.0880u [A]
M4 I_D	9.519398u [A]	10.4564u [A]
M1 g_m	188.0848u [A/V]	204.6989u [A/V]
M4 g_m	47.59699u [A/V]	52.3828u [A/V]
M1 g_{ds}	4.702120u [A/V]	4.5614u [A/V]
M4 g_{ds}	1.903880u [A/V]	1.6865u [A/V]

Table 1: Parameters of diode connection transistors

1.3.8 Error calculation SPICE vs MATLAB results

```
id1_calc=4.702120*10^-5;   %[A]
id1_spice=51.0880*10^-6;   %[A]
gm1_calc=1.880848*10^-4;   %[A/V]
gm1_spice=204.6989*10^-6;  %[A/V]
gds1_calc=4.702120*10^-6;  %[A/V]
gds1_spice=4.5614*10^-6;   %[A/V]
id4_calc=9.519398*10^-6;   %[A]
id4_spice=10.4564*10^-6;   %[A]
gm4_calc=4.759699*10^-5;   %[A/V]
gm4_spice=52.3828*10^-6;   %[A/V]
gds4_calc=1.903880*10^-6;  %[A/V]
gds4_spice=1.6865*10^-6;   %[A/V]

id1_percentage_error_result=id1_percentage_error_function(id1_calc,id1_spice);
fprintf('M1 current percentage error id1_error=%d%% \n',id1_percentage_error_result);
gm1_percentage_error_result=gm1_percentage_error_function(gm1_calc,gm1_spice);
fprintf('M1 transconductance percentage error gm1_error=%d%%
\n',gm1_percentage_error_result);
gds1_percentage_error_result=gds1_percentage_error_function(gds1_calc,gds1_spice);
fprintf('M1 output conductance percentage error
gds1_error=%d%%\n',gds1_percentage_error_result);
```

```
id4_percentage_error_result=id4_percentage_error_function(id4_calc,id4_spice);
fprintf('M4 current percentage error id4_error=%d%% \n',id4_percentage_error_result);
gm4_percentage_error_result=gm4_percentage_error_function(gm4_calc,gm4_spice);
fprintf('M4 transconductance percentage error gm4_error=%d%%
\n',gm4_percentage_error_result);
gds4_percentage_error_result=gds4_percentage_error_function(gds4_calc,gds4_spice);
fprintf('M4 output conductance percentage error gds4_error=%d%%
\n',gds4_percentage_error_result);

function id1_percentage_error_result=id1_percentage_error_function(id1_calc,id1_spice)
id1_percentage_error_result=abs((id1_calc-id1_spice)/id1_spice)*100;
end
function gm1_percentage_error_result=gm1_percentage_error_function(gm1_calc,gm1_spice)
gm1_percentage_error_result=abs((gm1_calc-gm1_spice)/gm1_spice)*100;
end
function
gds1_percentage_error_result=gds1_percentage_error_function(gds1_calc,gds1_spice)
gds1_percentage_error_result=abs((gds1_calc-gds1_spice)/gds1_spice)*100;
end
function id4_percentage_error_result=id4_percentage_error_function(id4_calc,id4_spice)
id4_percentage_error_result=abs((id4_calc-id4_spice)/id4_spice)*100;
end
function gm4_percentage_error_result=gm4_percentage_error_function(gm4_calc,gm4_spice)
gm4_percentage_error_result=abs((gm4_calc-gm4_spice)/gm4_spice)*100;
end
function
gds4_percentage_error_result=gds4_percentage_error_function(gds4_calc,gds4_spice)
gds4_percentage_error_result=abs((gds4_calc-gds4_spice)/gds4_spice)*100;
end
```

```
M1 current percentage error id1_error=7.960382e+00%
M1 transconductance percentage error gm1_error=8.116360e+00%
M1 output conductance percentage error gds1_error=3.085018e+00%
M4 current percentage error id4_error=8.961038e+00%
M4 transconductance percentage error gm4_error=9.136224e+00%
M4 output conductance percentage error gds4_error=1.288942e+01%
```

Code 9: Percent errors between calculated results and Spice simulation using MATLAB.

Finally based on code 9 we see that the results calculated with MATLAB have a small error from the ones calculated with SPICE. That can't be surprising because SPICE takes in consideration all the parameters of the level 1 technology.

2 CMOS IC Resistors Capacitors and Switches

Analog integrated circuit consist of passive components such as resistors, capacitors and switches. On this chapter we examine the construction of those passive components and the problems that might occur on a circuit.

2.1 Integrated Resistor Layouts

The most common way of IC resistor is the polysilicon resistor. There are also other structures such as N_implant diffusion that sits on top of the substrate and also P_implant diffusion that is inside the N_Well. In this section we will integrate a polysilicon resistor which is the most common because it confronts the shielding problem that other implementations are susceptible.

2.1.1 Polysilicon

The width and the length of resistor are defined by Poly layer. On top of the Poly layer we have the Resistor_ID layer in order to define the structure as a resistor. Figure 25 shows the resistivity of Poly layer. Equation 7 can be used to calculate the resistor by changing the width and length of the structure. Using code 10 and setting the appropriate parameter values which are width 0.34μm and length 25μm we construct a resistor of 308 ohm. Figure 26 shows the layout design of 308 ohm resistor constructed with Poly layer and two contacts. Figure 27 shows the cross-section of the resistor.

$$R = \frac{L}{W} R_{\square} \quad (7)$$

Figure 25: Electrical properties of polysilicon.

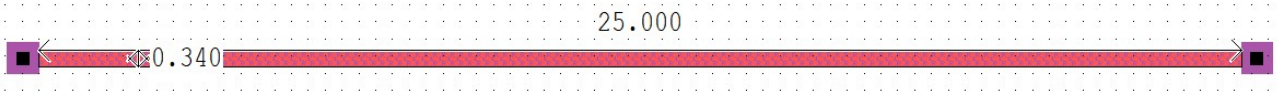


Figure 26: Layout of polysilicon resistor 308 ohm.

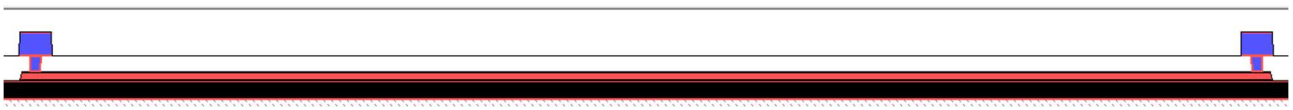


Figure 27: Cross-section of polysilicon resistor 308 ohm.

2.1.2 Serpentine structure using polysilicon

To design a resistor that has a value of several kohms it is advisable a structure like serpentine. That is because we can achieve large resistors but in a minimum space area. Designing a 1kΩ resistor with polysilicon on top of the substrate with sheet resistance 4.2 ohms/square. The width of the strips must be 1μm and the length of each strip 10μm long. Using the eq. 8 we calculate the number of squares needed.

$$R = R_{\square} N_{squares} \quad (8)$$

From eq. 8 the number of squares calculated are 238. Using code 11 which calculates the vertical squares based on total squares of the resistor and defines for this structure that vertical parts should be 8.

Figure 28: Electrical properties of polysilicon.

Figure 29 shows the serpentine structure of a 1kohm resistor made with Poly layer. The number of vertical, horizontal and total squares calculated using code 11. Figure 30 shows the cross-section of the 1kohm resistor.

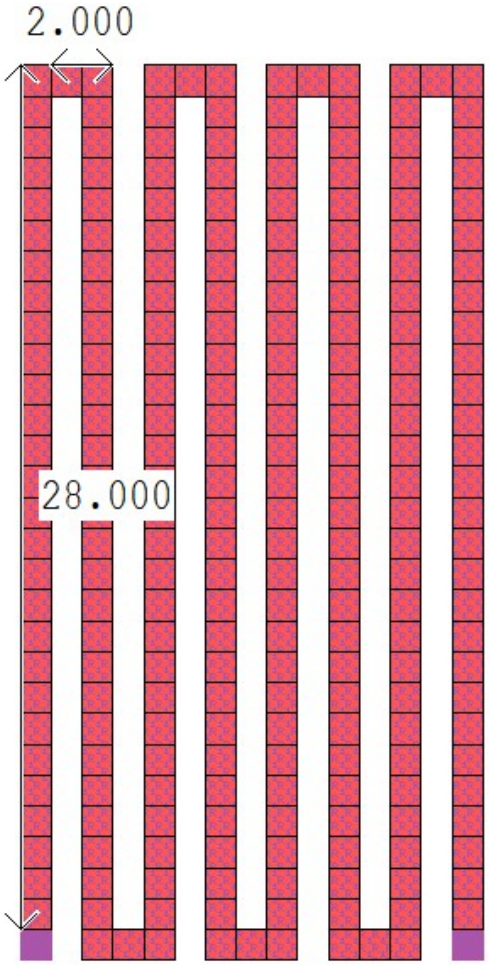


Figure 29: Serpentine structure of 1kohm resistor.

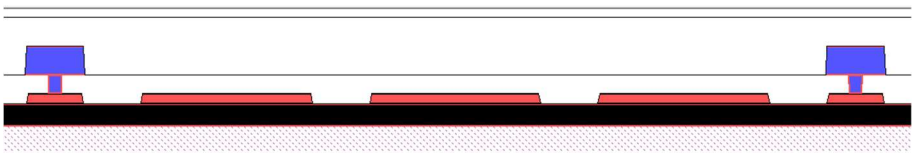


Figure 30: Cross-section of serpentine structure 1kohm resistor.

2.2 Integrated Capacitor Layouts

The most common way to fabricate a capacitor is using polysilicon and N_implant or P_implant diffusion. In this chapter we will design a polysilicon-N_implant capacitor.

2.2.1 Poly-diffusion capacitor

The polysilicon-N_implant capacitor is made with N_Implant on top of the substrate which is the bottom plate and a plate of polysilicon on top of the diffusion upper plate. The area that takes place under the polysilicon plate defines the capacitor value. To design a 2pF capacitor using the eq. 9 we must find the width and length of the structure. The shape of the capacitor will be square. Using SPICE model 0.35μm on SPICE files section 5.2. Code 12 used to calculate the oxide capacitance and then setting the needed width and length to achieve a 2pF capacitor. Figure 31 shows the layout design of a 2pF capacitor structured using Poly-N_implant layers. Figure 32 shows the cross section of the layout design.

$$C = \frac{\varepsilon_o \cdot \varepsilon_r}{T_{ox}} \cdot W \cdot L \quad (9)$$

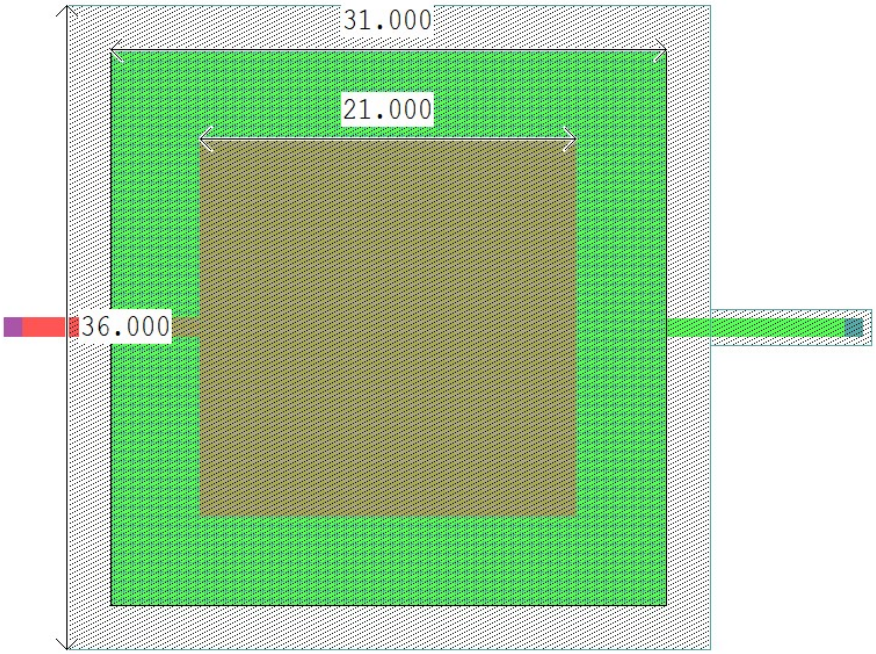


Figure 31: Layout of 2pF polysilicon-N_implant capacitor.

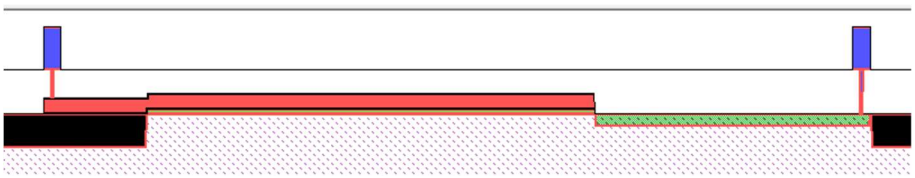


Figure 32: Cross-section of 2pF polysilicon-N_implant capacitor.

2.3 NMOS transistor Analog switch

A CMOS device can be used as a switch. Switches are important in analog applications because they transfer charge from one node to another. Applying a voltage at the gate of the transistor we can achieve the ON and OFF state of the device. In our case we use NMOS transistor. We apply a positive voltage for the ON state. Using Vp=3.3V at 1Mhz and input voltage Vin=1.3V at 2Mhz to charge the C1 capacitor as shown in (Fig. 33). M1 remains in the triode region when the gate voltage is higher than Vin and Vout by a value greater than Vth. The transistor is a variable resistor depending on the biasing. Resistance becomes maximum Ron_max when Vout≃Vin. Resistance becomes minimum Ron_min when Vin is zero or negative. Using SPICE level 1 0.5μm SPICE files section 5.1.

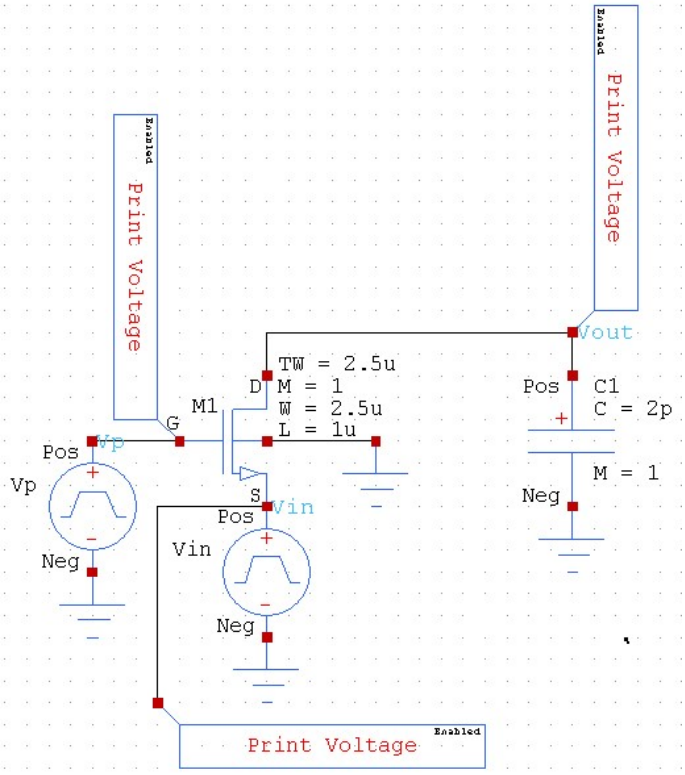


Figure 33: Schematic design of NMOS as switch.

2.3.1 On-Resistance calculation

Using code 13 we calculate the oxide capacitance for SPICE model level 1 0.5μm based on eq. 1. This parameter is useful for calculating the on-resistance of transistor. With eq. 10 and code 14 we calculate the maximum on-resistance. Using carrier mobility provided by SPICE parameters and oxide capacitance we calculate the process transconductance of our model using the eq. 2. Then with threshold voltage (Vth=700mV) provided by SPICE parameters the ON state of the transistor means gate voltage (Vp=3.3V) and source voltage (Vin=1.3V). We calculate the maximum resistance Ron_max=2.29kohm. Using the same parameters with code 14 and changing only the voltages of transistor for the OFF state that is source voltage (Vs=0V). We calculate the minimum on-resistance Ron_min=1.14kohm. Using eq. 11 we calculate the time constant for the circuit when operates in ON state. Using the Ron_max and the capacitor value we have a time constant TC=4.58ns calculated with code 16. In the transient analysis (Fig. 34) we see the charge and discharge of capacitor C1 based on circuit (Fig. 33). When applying a positive voltage Vp=3.3V at the gate Vout follows Vin. That's why we see a slight delay during the charging and discharging of C1.

$$R_{on} = \frac{1}{k_n \cdot W \cdot L \cdot (V_{gs} - V_{th})} \quad (10)$$

$$TC = R \cdot C \quad (11)$$

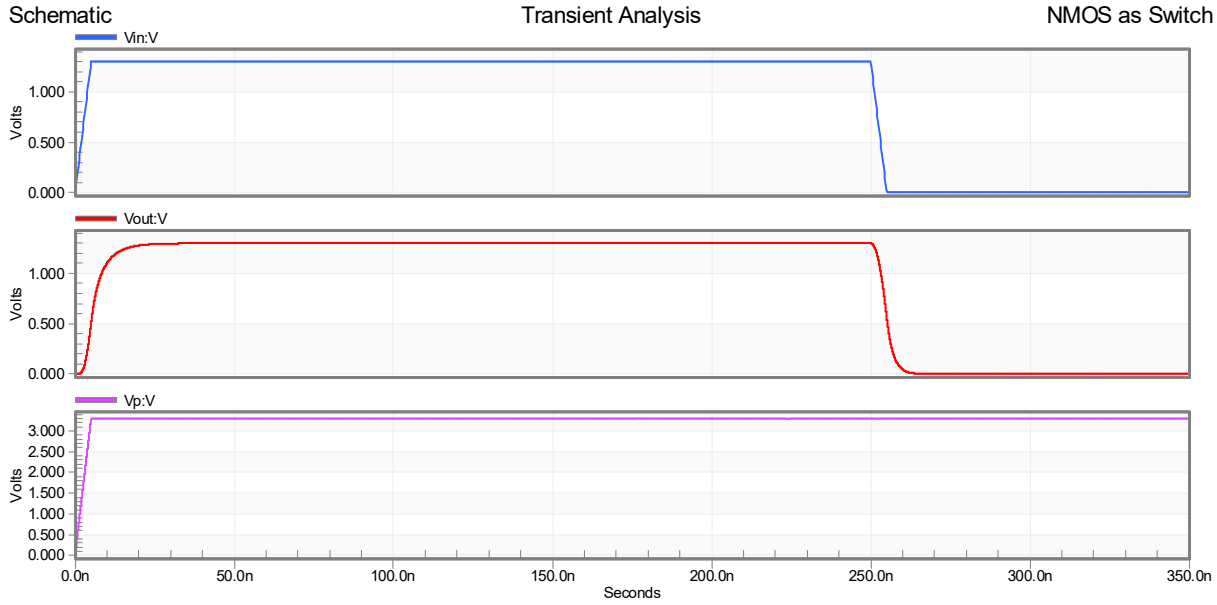


Figure 34: Transient analysis of charging and discharging a capacitor using NMOS.

2.3.2 Charge Injection

To understand the phenomenon of charge injection we will use Vp=3.3V at 1Mhz and a constant dc input voltage Vin=1.3V to charge the capacitor C1 as shown in (Fig. 35).

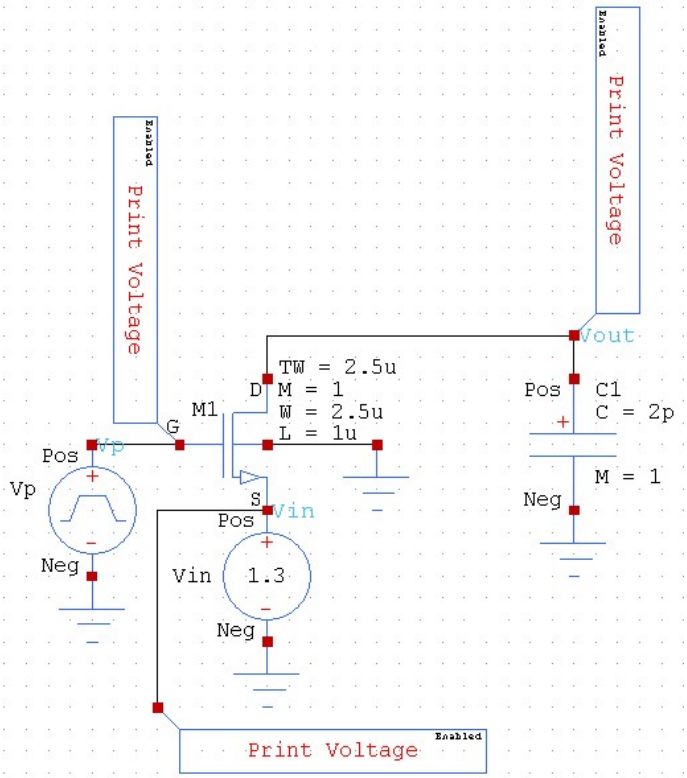


Figure 35: Schematic design NMOS for charge injection.

In the transient analysis (Fig. 36) we observe that when the clock of Vp goes OFF we have a voltage drop measuring the output node. The approximate value of this drop voltage is 5.9630mV as measured in (Fig 37). This mainly results because of the gate transition from ON to OFF state. When the switch goes OFF (Vp=0V) charges that are stored beneath the gate will be injected to drain or source so they don't charge the capacitor effectively. This may be a problem when we need to read the voltage of capacitor in another circuit and it's not accurately the voltage we need. Figure 36 shows more in detail the phenomenon that occurs with charge injection by zooming in as shown in (Fig. 37).

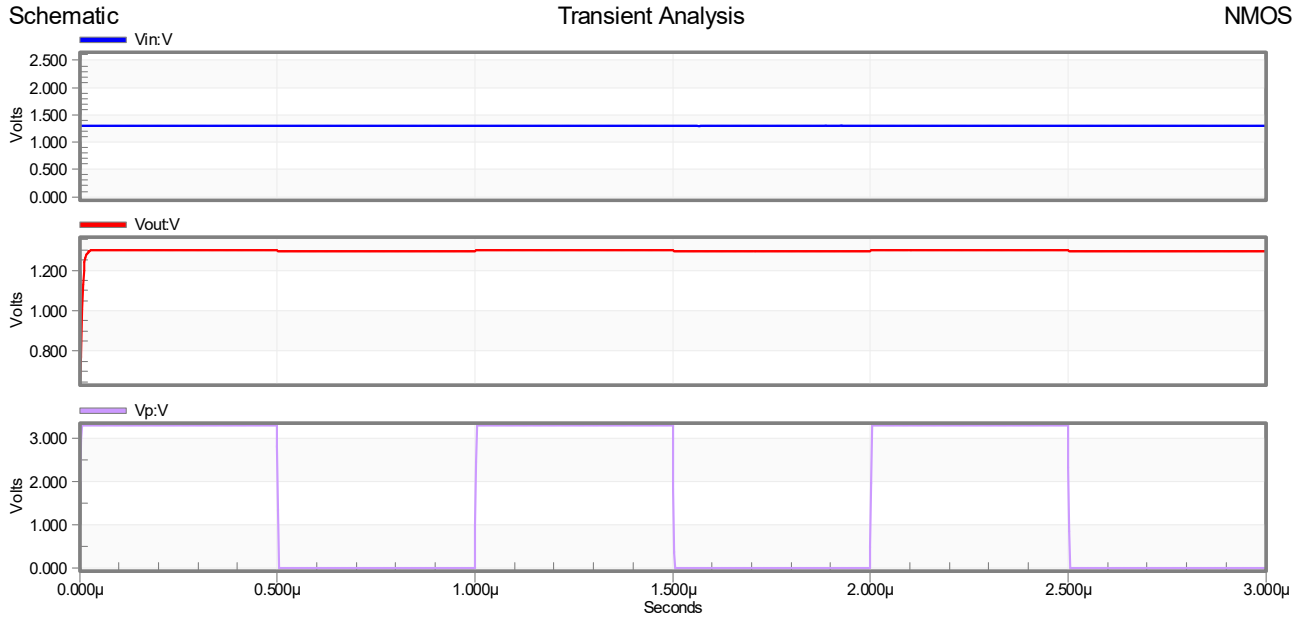


Figure 36: Transient analysis of charge injection.

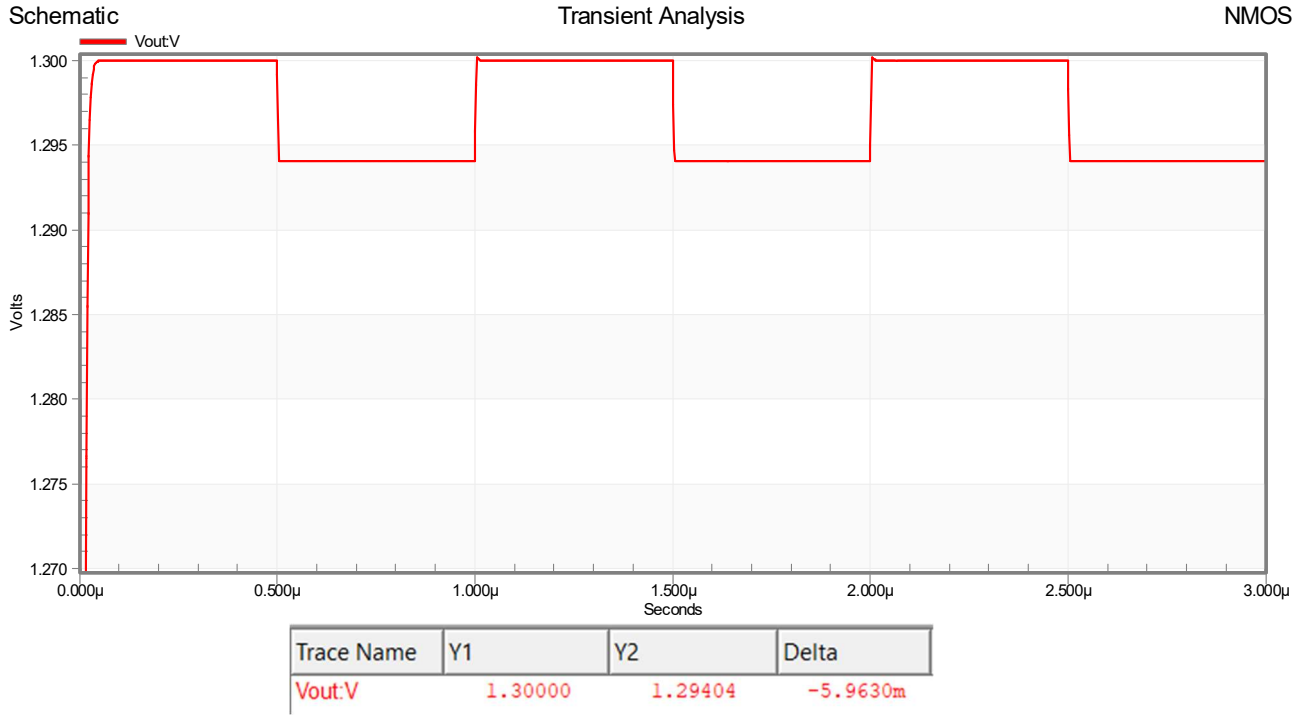


Figure 37: Output behavior of charge injection.

2.3.3 Channel charge calculation

$$Q_{ch} = W \cdot L \cdot C_{ox} \cdot (V_g - V_s - V_{th}) \quad (12)$$

By using eq. 12 and code 17 we manage to calculate the charge that is stored inside the channel of NMOS transistor. The parameters such as oxide capacitance, width, length, threshold voltage and gate voltage are the same with previous section 2.3.1. The source voltage equals to 1.3V. The charge stored in the channel of NMOS transistor in ON state is Qch_Ntype=12.5f Coulomb. When the transistor is turned OFF, the charges of the channel that are keeping the capacitor in 1.3V return to source so we have a drop voltage. That's why the phenomenon of charge injection appears. In the next section we will study circuits that can possibly reduce this drop voltage that is been created by charge injection.

2.4 Charge injection alleviating circuits

The charge injection can result in considerable errors particularly for high resolution data converters that require accuracy. Generally it is difficult to alleviate this error but there are some methods that can be used and have better results.

2.4.1 Dummy switch

A common and simple way to cancel the effect of charge injection is the dummy switch. Using two NMOS transistors in series and one connected to the capacitor having source and drain terminals sorted. In (Fig. 38) the width of M1 is advisable two times larger than M2 in order to achieve a low on-resistance and having small time constant for quick charging. The clock of dummy switch transistor M2, acts when clock of M1 goes OFF. We use the same frequency for both pulses. When the clock of M1 goes OFF half of the channel charge is injected towards M2. Then M2 goes ON and the channel charge under the gate matches the charge that has been induced from M1. V1=3.3V at 1Mhz, V2=3.3V at 1Mhz and Vin=1.3V.

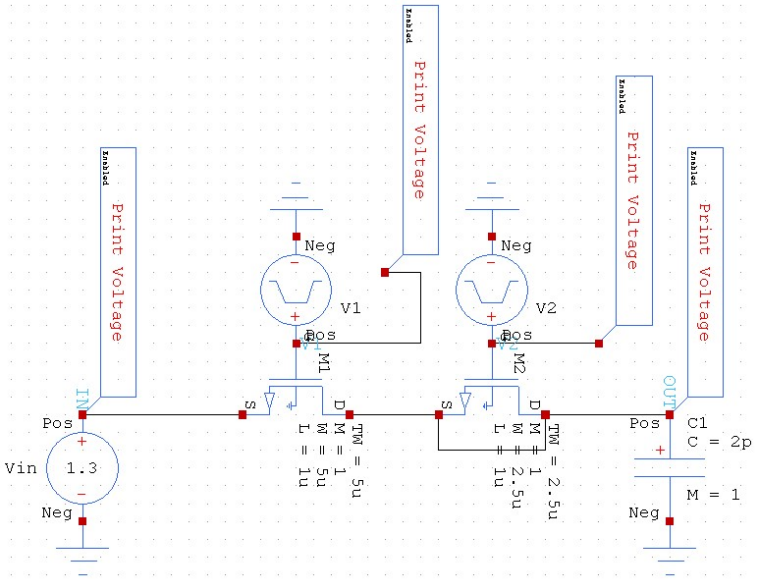
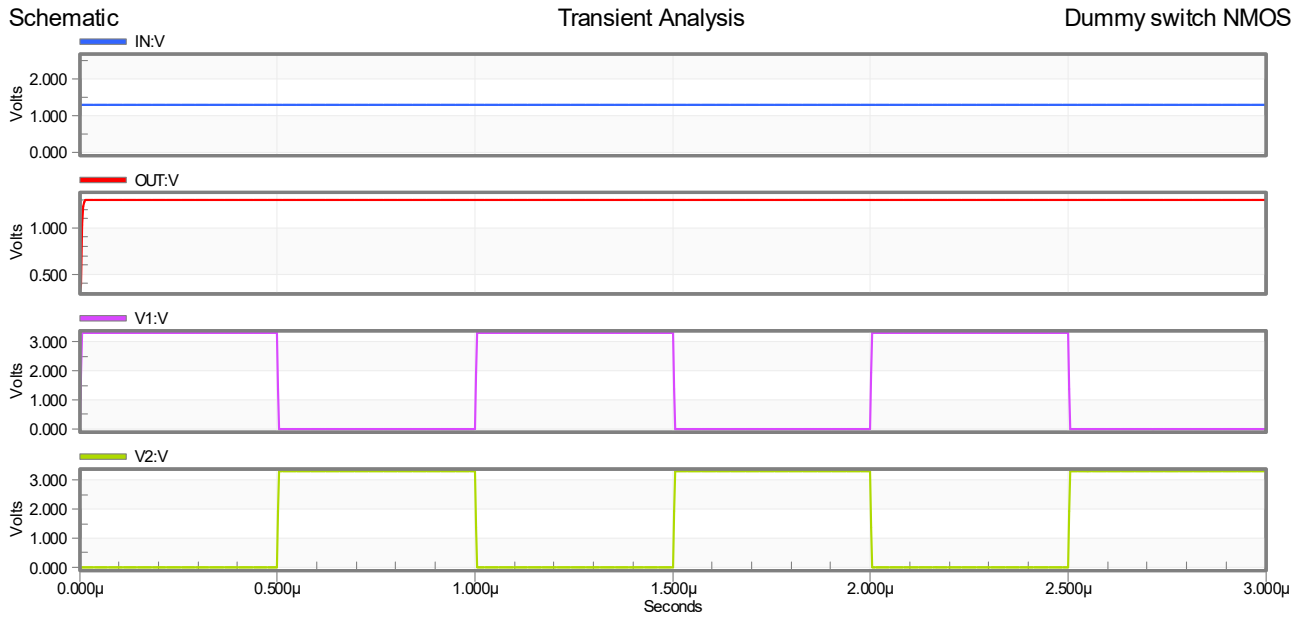


Figure 38: Schematic design of dummy switch.

In transient analysis (Fig. 39) we observe the complementary phase of voltage sources for transistor M1 and M2. By looking the trace voltage at the output node (OUT) (Fig. 39) we can see a drop of voltage about 368.561μV. It is clear now that with the method of dummy switch we have reduced the drop voltage error in a significant way.



Trace Name	Y1	Y2	Delta
IN:V	1.3	1.30	0.000
OUT:V	1.3	1.30	-368.561u
V1:V	3.3	0.00	-3.300
V2:V	0.0	3.30	3.300

Figure 39: Transient analysis of dummy switch.

2.4.2 Parallel transistors

Parallel transistors is another way to use. V1=3.3V at 1Mhz and V2=3.3V at 1Mhz with phase shift of 500ns. By using the same aspect ratio we ensure same Ron-resistance. With complementary phase shift and same Ron-resistance we manage to have smooth transition from ON to OFF state between the two transistors. By looking node (OUT) and trace voltages of the transient analysis (Fig. 41) we can see that there is no drop voltage. In other words, the effect of charge injection has been solved.

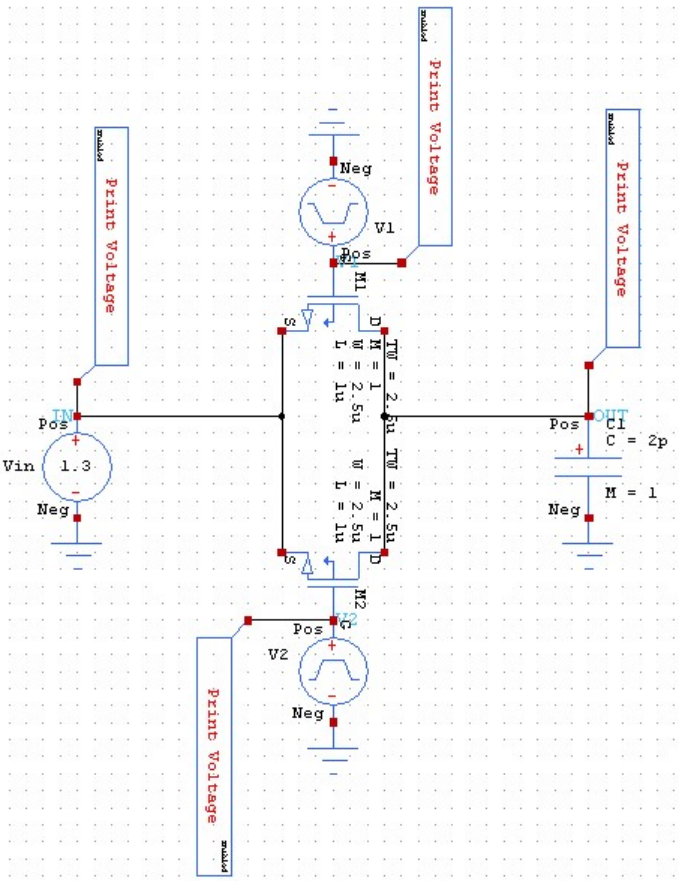
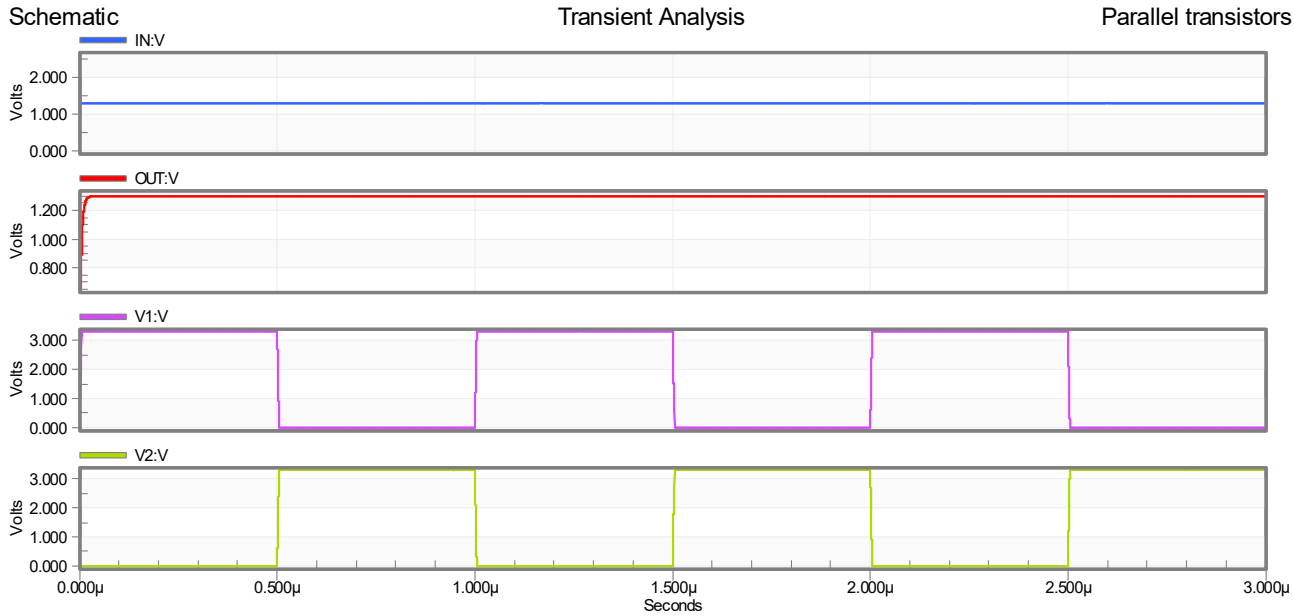


Figure 40: Schematic design of parallel transistors.



Trace Name	Y1	Y2	Delta
IN:V	1.3	1.3	0.0000
OUT:V	1.3	1.3	0.0000
V1:V	3.3	0.0	-3.3000
V2:V	0.0	3.3	3.3000

Figure 41: Transient analysis of parallel transistors.

3 Building Blocks

In analog systems, operational amplifiers can be designed with some basic building blocks, such as simple gain stages, differential pairs and differential to single ended convertors. In this chapter we will design some of these building blocks according to general performance soecifications. We will present AC, DC and transient analysis simulations of the designed blocks.

3.1 Push-Pull Inverter

Figure 42 shows the schematic design of a push-pull inverter and Fig. 43 shows its layout. To design it as efficient as possible is recommended that PMOS transistor should have two times larger width than NMOS. Keep in mind that $\mu_n \cong 2 \cdot \mu_p$ and since the gates are connected you want to have the same charging rate at the input. Choosing the device aspect ratio for the PMOS and NMOS transistor this circuit can operate as an amplifier. Both transistors are being driven by the same input. One of the advantages of push-pull configuration is that the output swing operates close to VDD and GND. Verification shows that design and layout are equal.

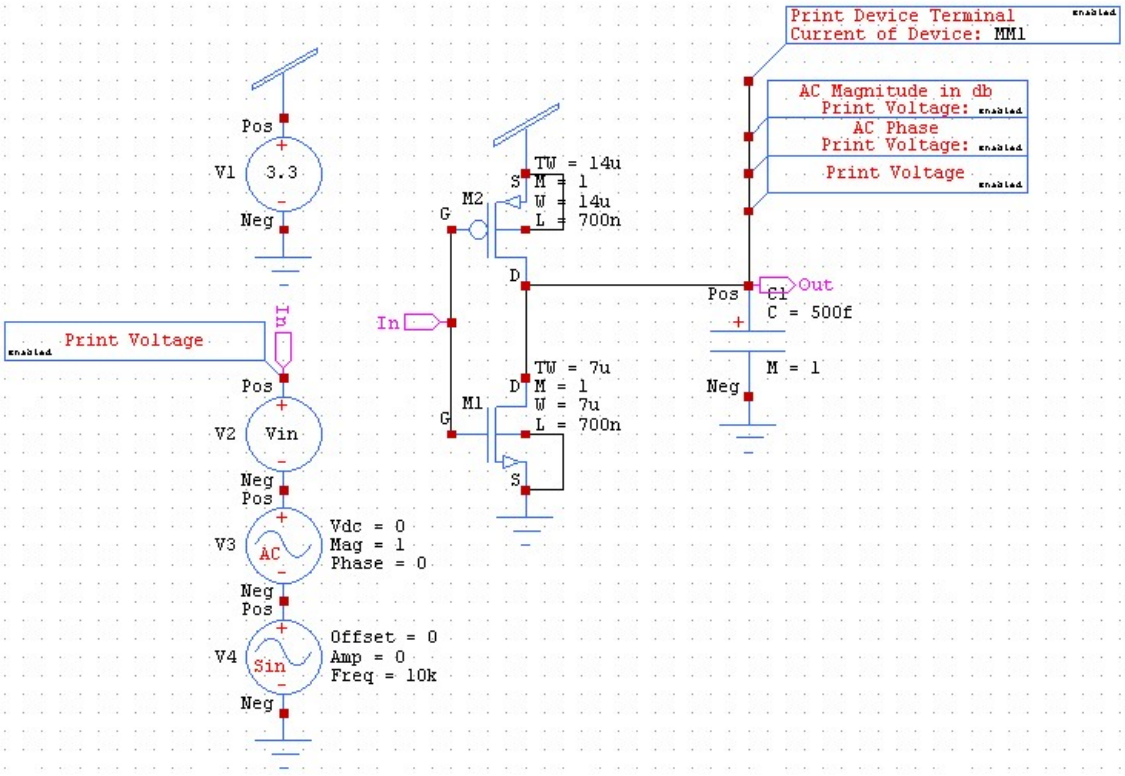


Figure 42: Schematic design of push-pull inverter.

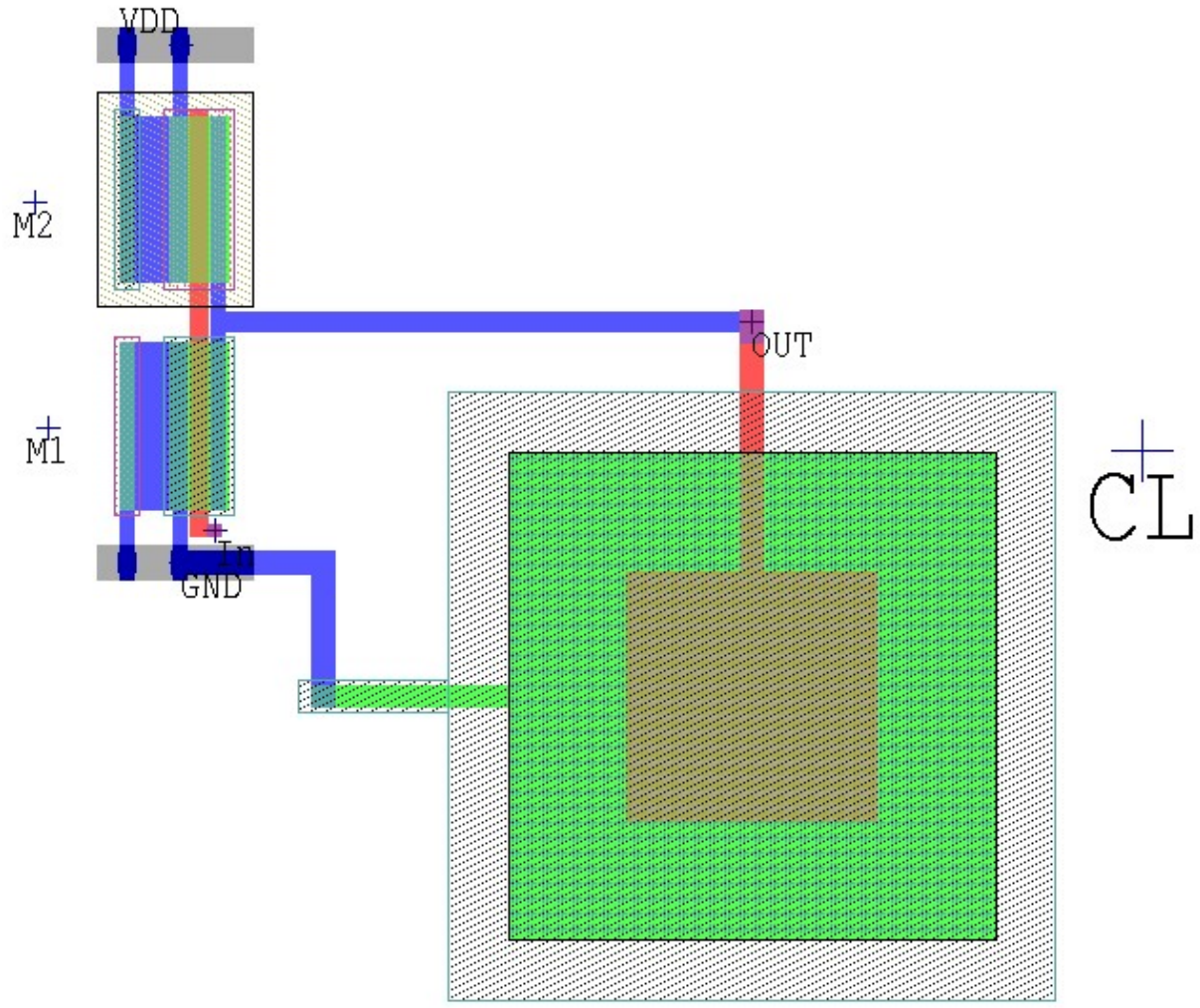


Figure 43: Layout design of push-pull inverter.

Figure 44 shows the voltage transfer characteristic and the drain current of push-pull inverter, at the biasing point where Vin=Vout and also the current value at that point. This characteristic is important for the designer to see the output voltage range that push-pull inverter can achieve. At the biasing point we can see clearly that we have the maximum current. For an amplifier one of the basic characteristics is the output voltage swing and gain. From the VTC characteristic when the slope $\frac{dV_{out}}{dV_{in}} = -1$ shows the maximum and the minimum swing that the amplifier can achieve without distorting the signal. By biasing the circuit on point Q where Vin=Vout we can achieve the maximum output swing VOH and VOL.

- VOH: VDD=3.3V, Vin=863mV, Vout= 3.146V NMOS(saturation), PMOS(triode).
- VOL:VDD-3.3V, Vin=1.395V, Vout=298.17mV NMOS(triode), PMOS(saturation).

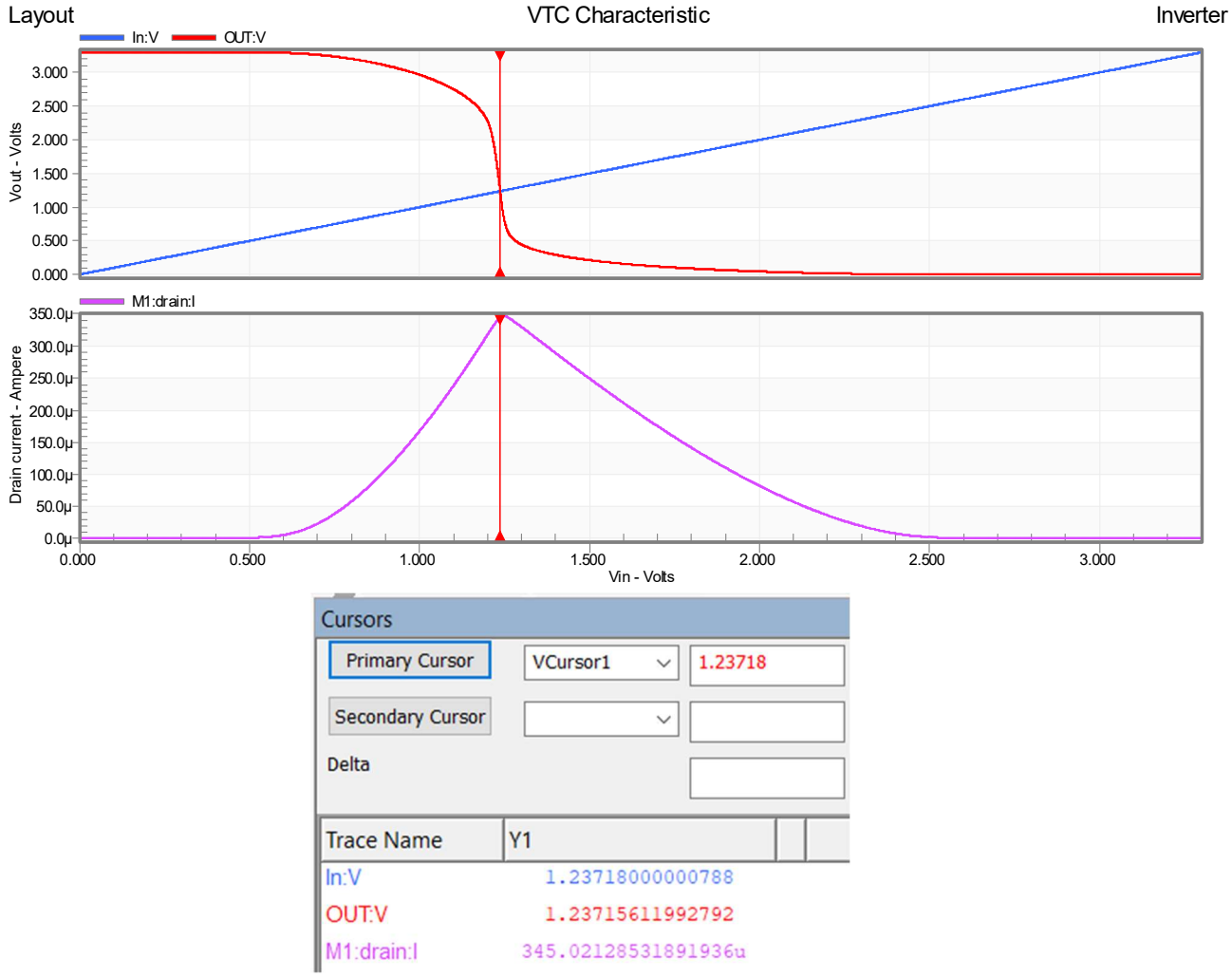


Figure 44: Biasing point of push-pull inverter.

Figure 45 shows the different input-output characteristics for different power supply voltages. When the power supply voltage increases the output voltage range increases as well and the biasing point of the maximum gain changes. The importance of the input-output characteristic for different supply voltage provides details about the changes in range of output swing.

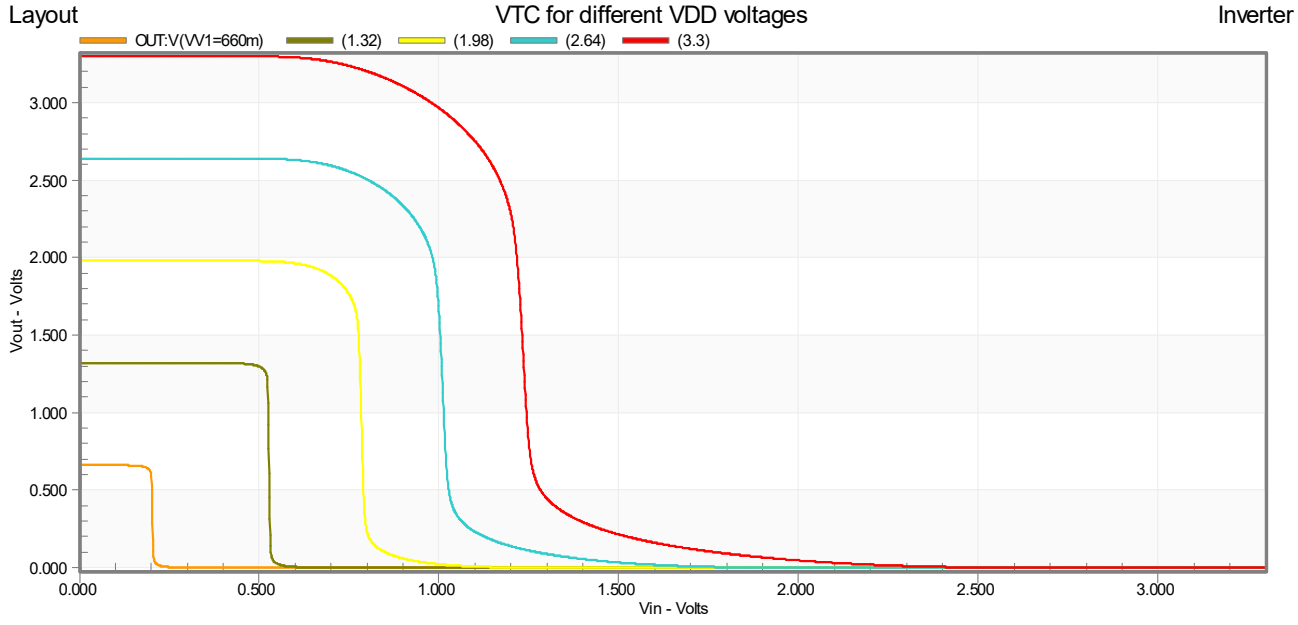
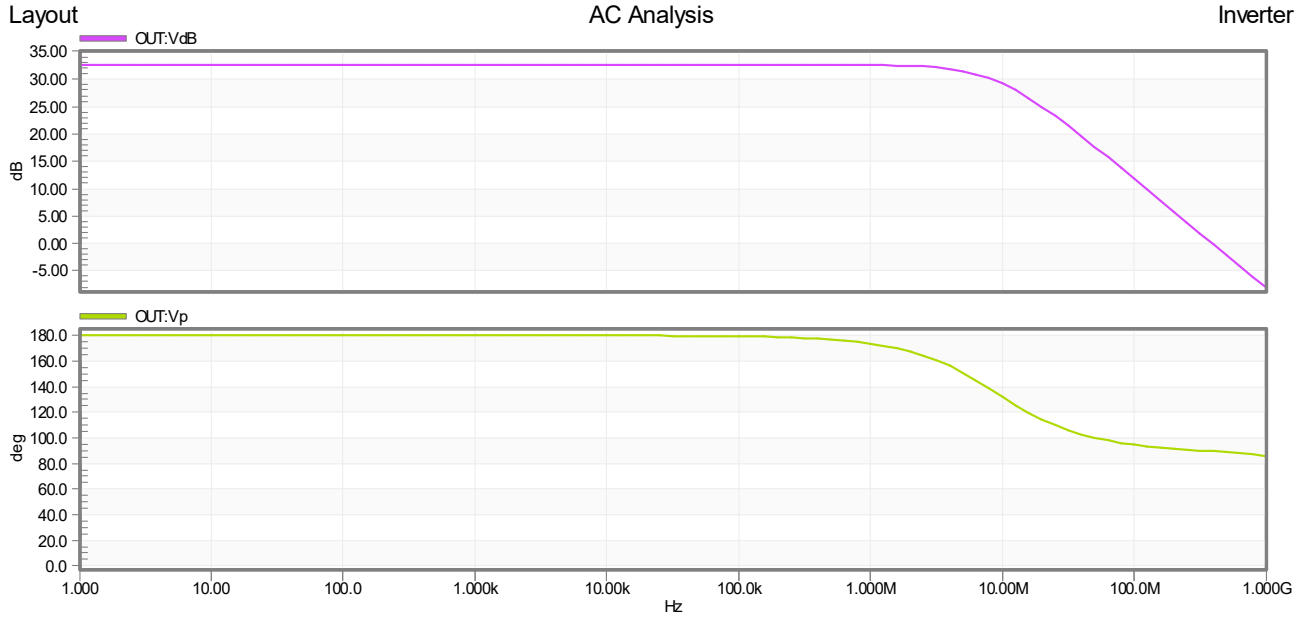


Figure 45: Voltage transfer characteristic sweeping the power supply voltage.

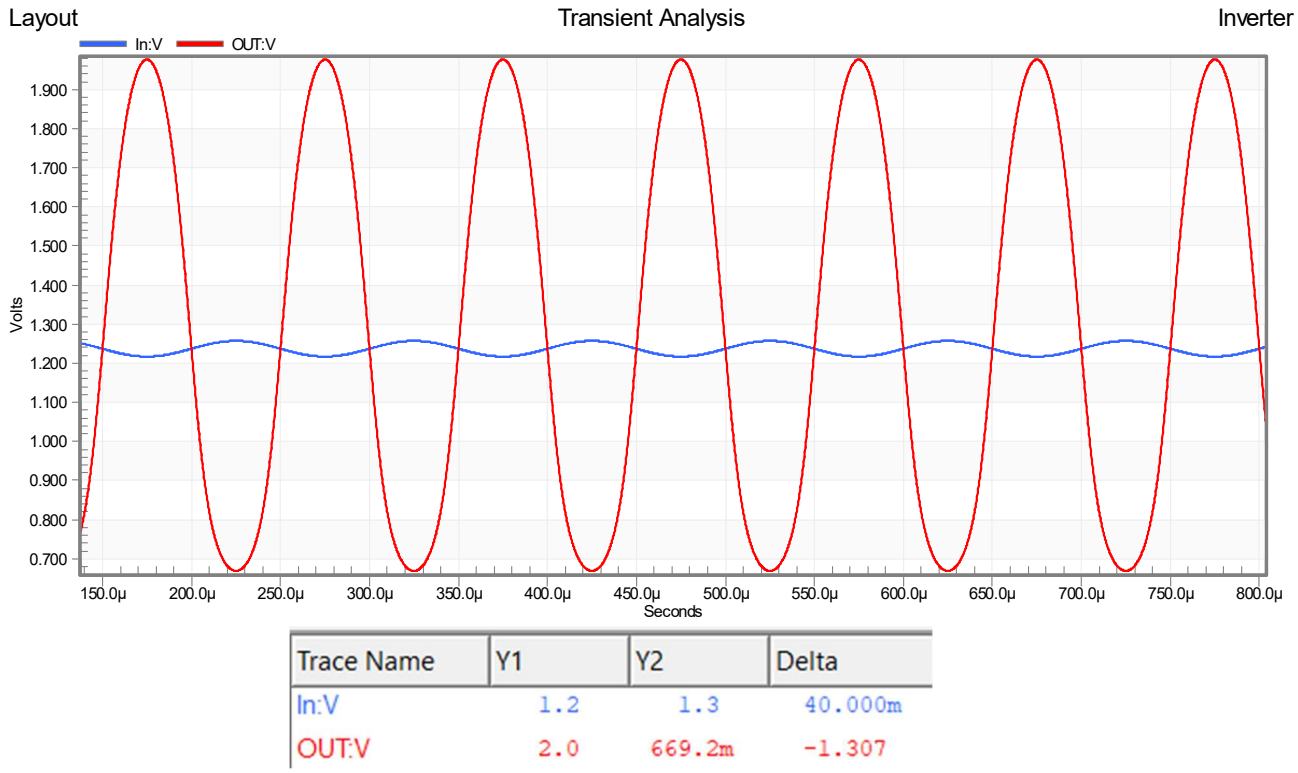
Figure 46 shows the AC analysis of push pull inverter. The circuit has a maximum gain around 32dB or Av=40. The unity gain bandwidth (ft) of the amplifier is around 391Mhz and this can be found when the characteristic of gain reaches 0dB. At 0dB the unity gain bandwidth frequency provides us information about the phase margin (PM). More specifically at 391Mhz on phase characteristic we have around 89° phase margin. Those calculations are important to determine whether the amplifier is stable or unstable. Because the phase margin is above 45° this means that the system is stable and in the output response we have no ringing. The bandwidth of the amplifier is determined by the -3dB which is the dominant pole at frequency of 9Mhz as shown in (Fig. 46). The theoretical calculations using MATLAB (code 19) based on (Netlist 9) are in close agreement (Fig. 46).




```
Measurement result summary
   Av_dB              =   32.6741
   PM                 =   89.4665
   ft                 =  391.1986MEG
   minus_threedb_pole =    9.0507MEG
```

Figure 46: AC analysis of push-pull inverter.

Figure 47 shows the transient analysis of push-pull inverter. By looking the peak to peak output trace voltage of transient analysis we see that the input signal is amplified as many times as the gain we extracted before.



Trace Name	Y1	Y2	Delta
In:V	1.2	1.3	40.000m
OUT:V	2.0	669.2m	-1.307

Figure 47: Transient analysis of push-pull inverter.

3.2 Inverter with Active Load

One of the simplest forms of gain stage is the inverter with active load. The difference from digital and push-pull inverters is that the input signal is applied to only one transistor. The gate of complementary transistor PMOS is biased with a fixed voltage and operates as an active load. A fixed voltage for the complementary transistor can be achieved with a diode connected transistor carrying a given bias current from a current source. The circuit to operate correctly, all the transistors must be in saturation region. At table 2 we see the performance specifications to design the inverter with active load.

Performance Specifications	Desired Values
VDD (V)	3.3
Overall Gain (A_V) (dB)	40
Unity Gain Bandwidth (GBW) (Mhz)	≥140
Phase Margin (PM) (°)	≥60
Power Dissipation (P_{diss}) (mW)	0.2
Output Voltage Swing (V)	0.2-3.1
Slew Rate (V/μs)	20
Load Capacitance (C_L) (pF)	0.5

Table 2: Inverter with active load specifications.

We begin calculating the minimum allowed current using the slew rate.

$I_{bias} = \frac{20}{10^{-6}} \cdot 0.5 \cdot 10^{-12} = 10\mu A.$

Next from the power dissipation we calculate the maximum allowed current for the circuit.

$P_{diss} = V_{DD} \cdot I_{bias} \rightarrow I_{bias} = \frac{0.2mW}{3.3V} = 60\mu A.$

Finally we use $I_{bias} = 30\mu A$ which is enough to ensure some margin.
Figure 48 shows the test transistors in order to choose the appropriate pair. All transistors have aspect ratio 10. With a first look on NMOS transistors MNtest and MNtest1. The one with the minimum length has higher transconductance value and also a lower overdrive voltage. These two parameters are important for our calculations for our next step considering the lower output swing and gain. Next we look at the pair of PMOS transistors MPtest and MPtest1. Considering that PMOS transistor will be our load we want a low output conductance. That is MPtest1 where has larger gate length. Figure 49 shows the initial small signal parameters of transistors.

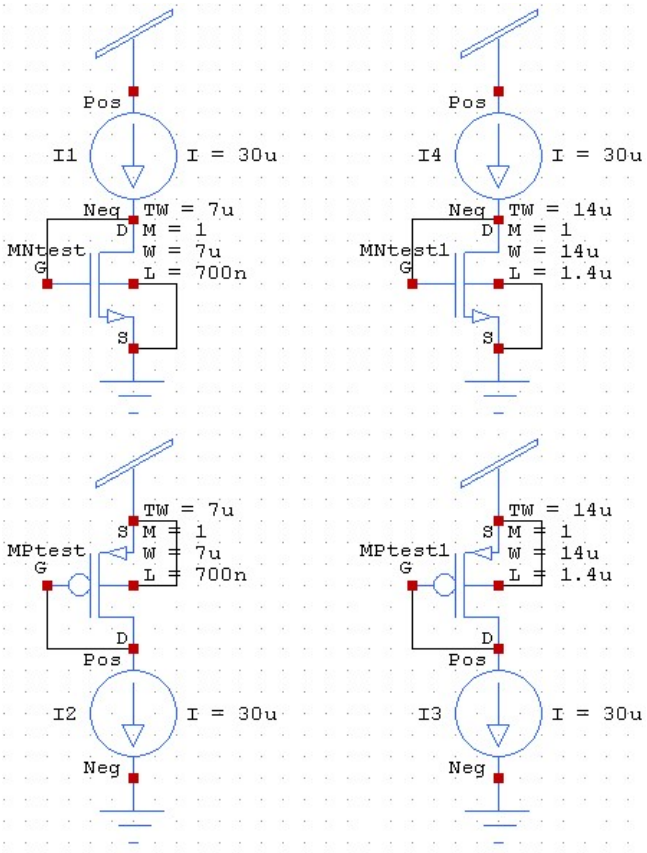


Figure 48: Schematic design transistors with initial aspect ratios.

	0	1	2	3
	MMNtest	MMNtest1	MMPtest	MMPtest1
MODEL	MODN	MODN	MODP	MODP
TYPE	NMOS	NMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	30.0000u	30.0000u	-30.0000u	-30.0000u
IBS	0.	0.	0.	0.
IBD	-586.3869a	-1.0733f	528.3124a	982.7928a
VGS	733.3162m	711.4370m	-1.0971	-1.0802
VDS	733.3162m	711.4370m	-1.0971	-1.0802
VBS	0.	0.	0.	0.
VTH	567.2290m	532.5964m	-791.0413m	-767.7440m
VDSAT	175.1087m	175.8738m	-303.8356m	-304.0723m
BETA	1.8860m	1.8374m	605.9361u	609.4053u
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	305.9780u	297.7112u	167.9245u	170.4255u
GDS	1.3761u	1.1167u	3.2751u	1.7295u
GMB	94.8500u	91.6415u	35.3237u	36.8273u
GBD	799.6371a	1.5087f	481.5652a	909.8164a
GBS	799.6371a	1.5087f	481.5652a	909.8164a
CDTOT	11.6878f	22.8563f	11.7823f	23.2200f
CGTOT	19.4029f	73.0347f	19.0108f	70.9615f
CSTOT	21.5932f	61.8459f	23.2784f	63.7541f
CBTOT	25.9907f	63.3124f	26.4946f	60.7604f
CGS	15.7608f	62.8845f	15.6608f	62.3211f
CGD	2.2107f	4.4073f	2.3905f	4.7898f
CGB	1.4314f	5.7429f	959.4666a	3.8505f
CBD	9.4743f	18.4540f	9.3795f	18.4313f
CBS	11.0065f	21.4154f	13.5790f	26.6236f

Figure 49: SPICE result of inverter with active load initial aspect ratios.

The bias current is 30μA. We chose a gate length $L_n = 0.7\mu m$ for NMOS transistor and for PMOS transistor $L_p = 1.4\mu m$. Remembering from specifications that we want an overdrive voltage close to 0.2V for both NMOS and PMOS transistors. Increasing the width of the MPtest1 we observe that the output conductance (gds) doesn't change a lot. So we stop increasing the width when we achieve an overdrive voltage 0.218V, this is shown in (Fig. 52). To achieve the required gain we need to increase the width of the input transistor MNtest. By doing this we increase the transconductance (gm). Using equation $g_m = 2\pi f_T C_L = 2\pi \cdot 140 \cdot 10^6 \cdot 0.5 \cdot 10^{-1} = 439.82\mu S$ we see that we need transconductance better than 439.82μS. This is achieved with $W_n = 35\mu m$ where $g_m = 525.16\mu S$ to ensure some margin for the unity gain frequency. The dc biasing voltage for MNtest=M1 is VGS1=604.8412mV. The final SPICE results are shown in (Fig. 50). Figure 51 shows the schematic design of inverter with active load and Fig. 52 shows its layout.

AC SMALL-SIGNAL MODELS: temperature=25.0

	0	1
	MMNtest	MMPtest1
MODEL	MODN	MODP
TYPE	NMOS	PMOS
REGION	Saturation	Saturation
ID	30.0000u	-30.0000u
IBS	0.	0.
IBD	-2.1991f	1.7015f
VGS	604.8412m	-963.3126m
VDS	604.8412m	-963.3126m
VBS	0.	0.
VTH	558.2332m	-756.8840m
VDSAT	94.6266m	-218.1932m
BETA	9.6110m	1.2680m
RS	0.	0.
RD	0.	0.
GM	525.1632u	247.0998u
GDS	1.7037u	1.9650u
GMB	163.4200u	53.4375u
GBD	3.6359f	1.7663f
GBS	3.6359f	1.7663f
CDTOT	56.9568f	47.0520f
CGTOT	84.6195f	140.5856f
CSTOT	96.0093f	126.3712f
CBTOT	125.4103f	122.1326f
CGS	63.0102f	122.6342f
CGD	10.8679f	9.5237f
CGB	10.7414f	8.4277f
CBD	46.0770f	37.5292f
CBS	52.6422f	52.7129f

Figure 50: SPICE result of chosen aspect ratios to design the inverter with active load.

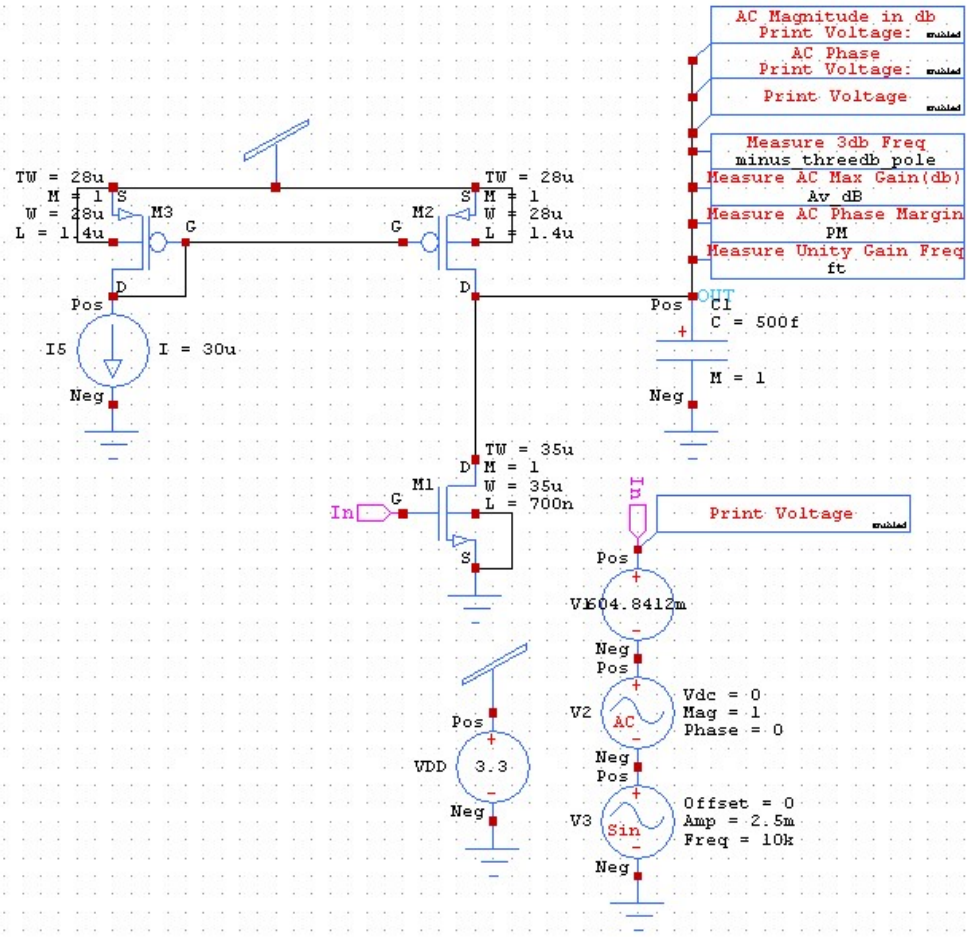


Figure 51: Schematic design of inverter with active load.

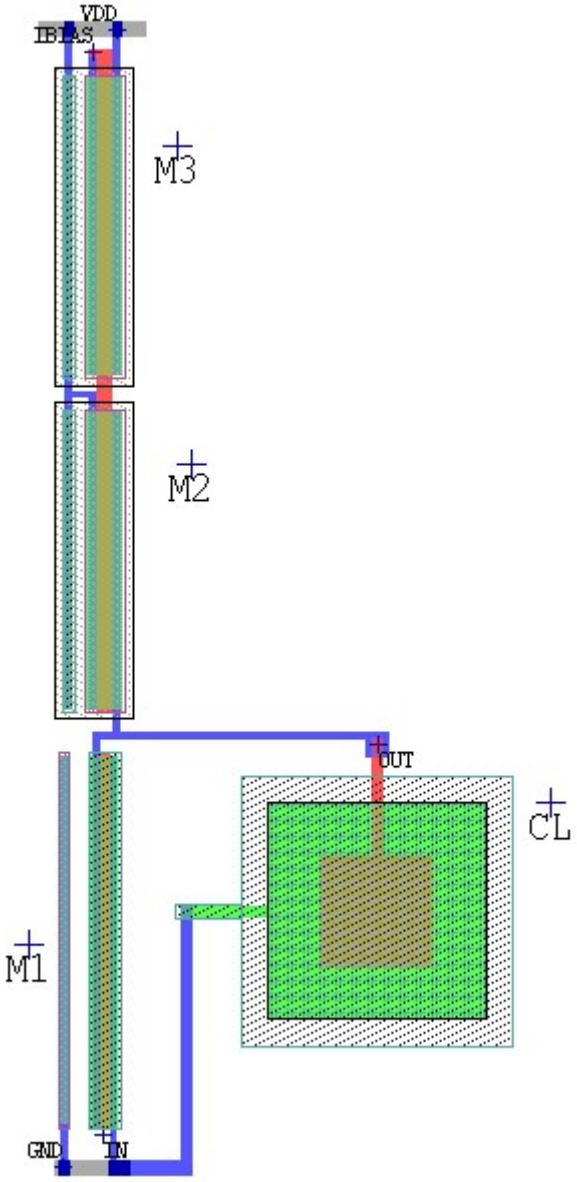


Figure 52: Layout design of inverter with active load.

Figure 53 shows the equivalent circuit of inverter with active load. The small signal parameters that we see on the circuit are calculated on APPENDIX A with code 20 using the small signal parameters of (Fig. 54).

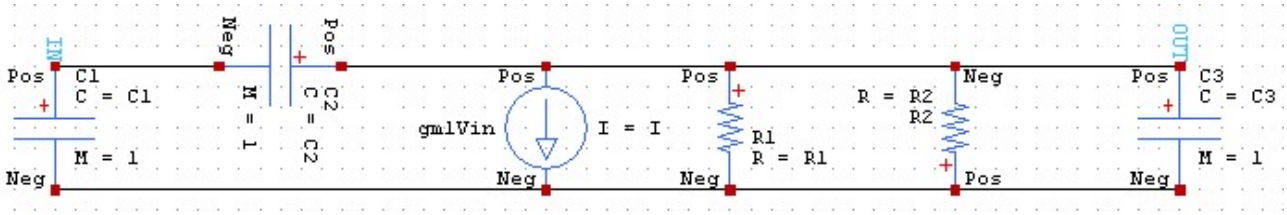


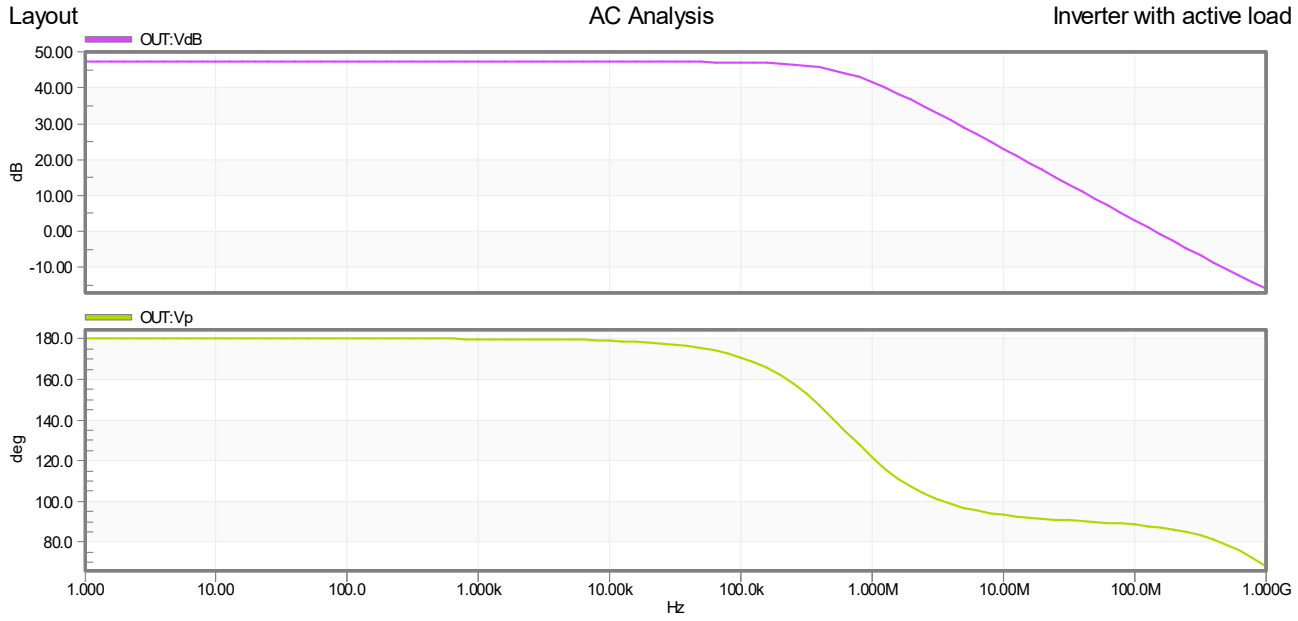
Figure 53: Equivalent circuit of inverter with active load.

AC SMALL-SIGNAL MODELS: temperature=25.0

	0	1	2
	M1	M2	M3
MODEL	MODN	MODP	MODP
TYPE	NMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation
ID	31.0705u	-31.0705u	-30.0000u
IBS	0.	0.	0.
IBD	-6.5096f	2.9809f	1.8398f
VGS	604.8412m	-963.3126m	-963.3126m
VDS	1.7392	-1.5608	-963.3126m
VBS	0.	0.	0.
VTH	557.1568m	-756.8175m	-756.8840m
VDSAT	95.2354m	-218.2483m	-218.1932m
BETA	9.6113m	1.2680m	1.2680m
RS	0.	0.	0.
RD	0.	0.	0.
GM	542.4882u	254.6113u	247.0998u
GDS	674.5822n	1.6723u	1.9650u
GMB	168.7803u	55.1008u	53.4375u
GBD	3.7428f	1.9099f	1.9099f
GBS	3.7428f	1.9099f	1.9099f
CDTOT	69.8388f	70.7717f	79.9971f
CGTOT	84.8332f	140.5498f	140.5856f
CSTOT	123.9540f	174.4697f	174.4900f
CBTOT	166.0771f	193.9778f	203.1965f
CGS	63.3038f	122.6074f	122.6342f
CGD	10.8594f	9.5084f	9.5237f
CGB	10.6700f	8.4340f	8.4277f
CBD	58.9654f	61.2600f	70.4743f
CBS	80.4113f	100.8317f	100.8317f

Figure 54: Small signal parameters of inverter with active load.

Figure 55 shows the AC analysis of inverter with active load. The circuit has a maximum gain around 47dB or Av=230. The unity gain bandwidth (ft) of the amplifier is around 145Mhz and this can be found when the characteristic of gain reaches 0dB. At 0dB the unity gain bandwidth frequency provides us information about the phase margin (PM). Because the phase margin is above 45° this means that the system is stable and in the output response we have no ringing. The bandwidth of the amplifier is determined by the -3dB which is the dominant pole at frequency of 616kHz as shown in (Fig. 55). The theoretical calculations using MATLAB (code 20) based on (Netlist 10) are in close agreement (Fig. 55).



```
Measurement result summary
   Av_dB                =    47.2781
   PM                   =    87.4007
   ft                   =  145.2320MEG
   minus_threedb_pole   =  615.9032k
```

Figure 55: AC analysis of inverter with active load.

Figure 56 shows the transient analysis of inverter with active load. By looking the trace voltage of transient analysis (Fig. 56) we see that the input signal is amplified as many times as the gain we extracted before. Figure 57 shows the power dissipation of inverter with active load around 0.2mW. Table 3 shows the desired and the achieved performance characteristics of the amplifier.

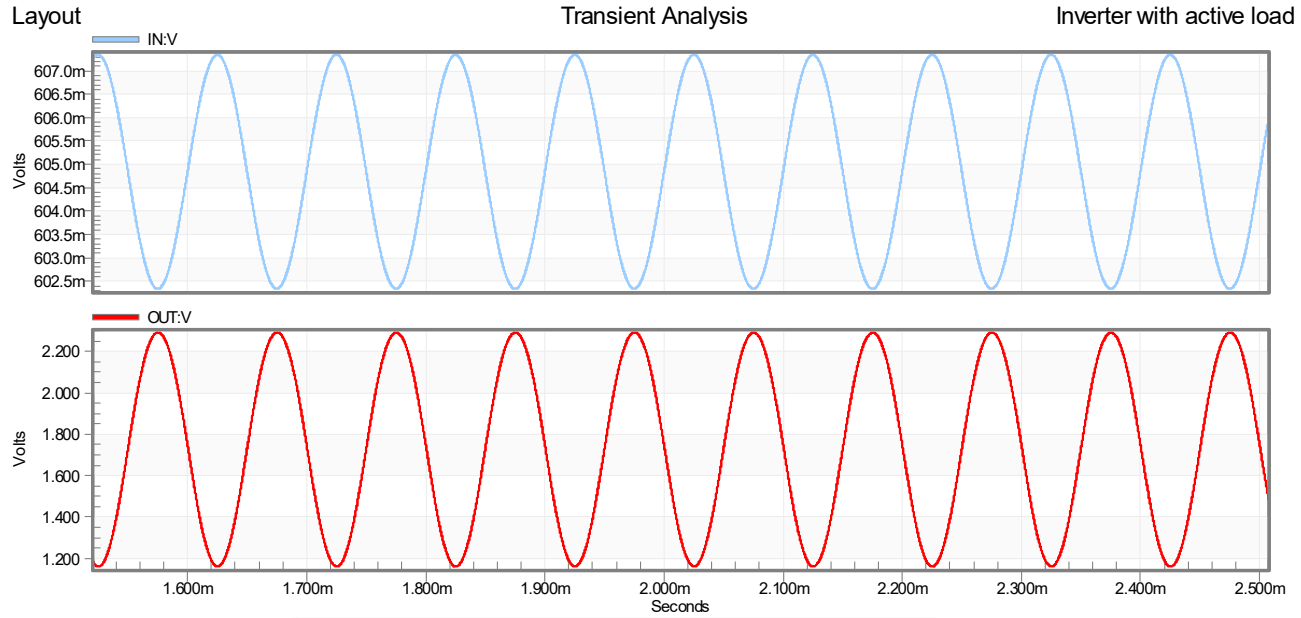


Figure 56: Transient analysis of inverter with active load

```
Average power consumed -> 2.014899e-04 watts
```

Figure 57: Power dissipation of inverter with active load.

Performance Specifications	Desired Values	Simulation Values
Overall Gain (A_V) (dB)	40	47
Unity Gain Bandwidth (GBW) (Mhz)	≥140	145
Phase Margin (PM) (°)	≥60	87
Output Voltage Swing (V)	0.2-3.1	0.094-3.1
Power Dissipation (P_{diss}) (mW)	0.2	0.2

Table 3: Performance results of inverter with active load.

3.3 Cascode with Active Load

The design of the cascode is same as inverter with active load but we add an extra NMOS transistor in series with the input transistor. It provides higher output impedance and decouples input from output reducing the Miller effect of capacitance. It is important to mention that all the transistor carry the same biasing and signal currents. All transistors must operate in saturation region in order the circuit to operate correctly.

Specifications are same as inverter with active load in order to see the changes that causes the cascode transistor. So we follow the same designing concept. Using 30uA current and 3.3V on our supply voltage. Then we find the biasing voltages for M1 and M2 with diode connection configurations. Dc bias input voltage of M1 is 604.8412mV and for M2 is VB=VDS1+VGS1=1.3733V, this is shown in (Fig. 58) applied on the dc voltage sources. Figure 58 shows the schematic design of cascode with active load and Fig. 59 shows its layout.

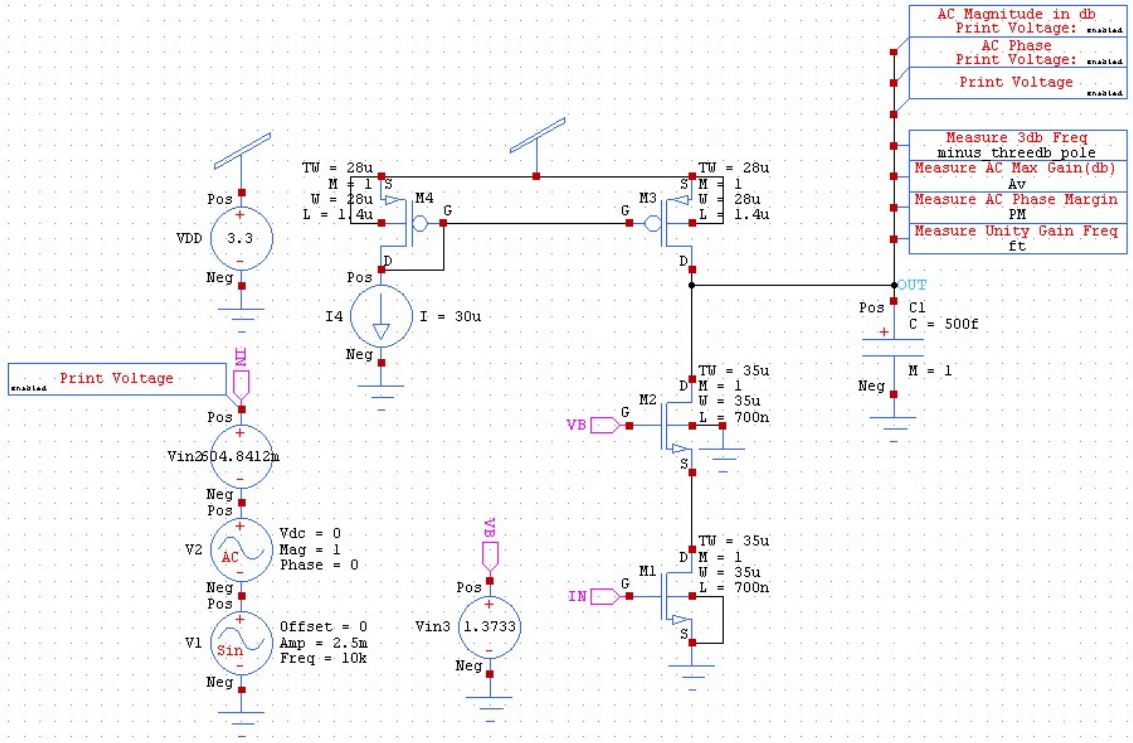


Figure 58: Schematic design of cascode with active load.

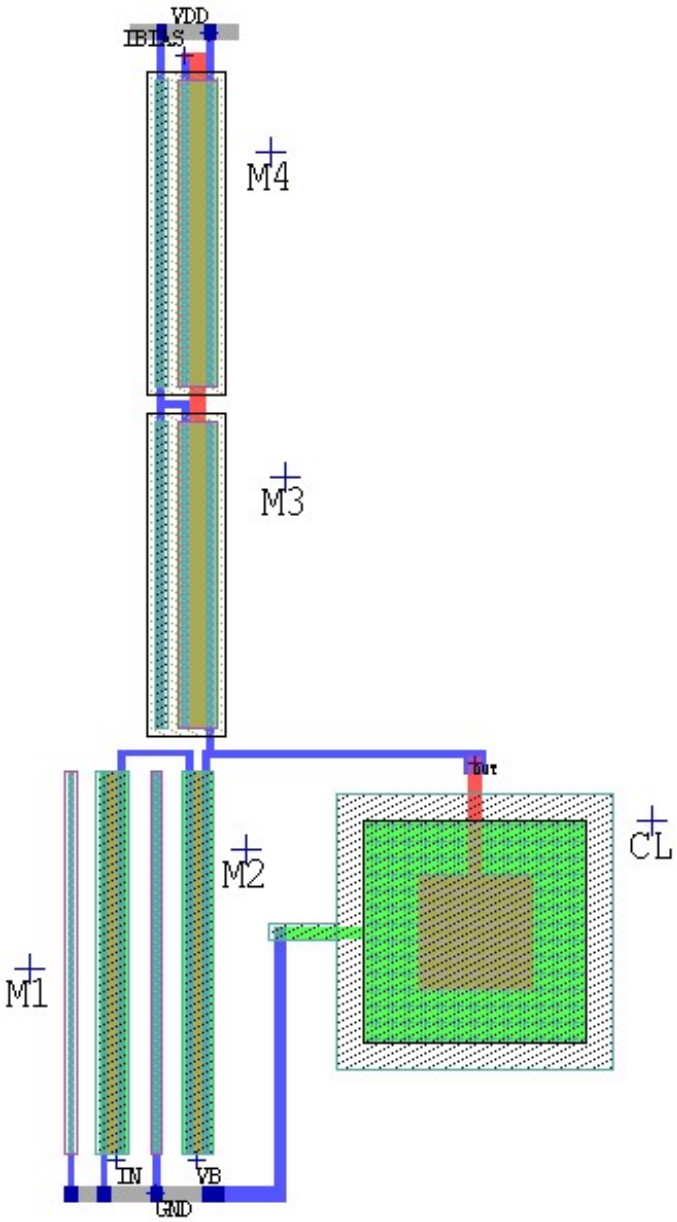


Figure 59: Layout design of cascode with active load.

Figure 60 shows the equivalent circuit of cascode with active load. The small signal parameters that we see on the circuit are calculated on APPENDIX A with code 21 using the small signal parameters of (Fig. 61).

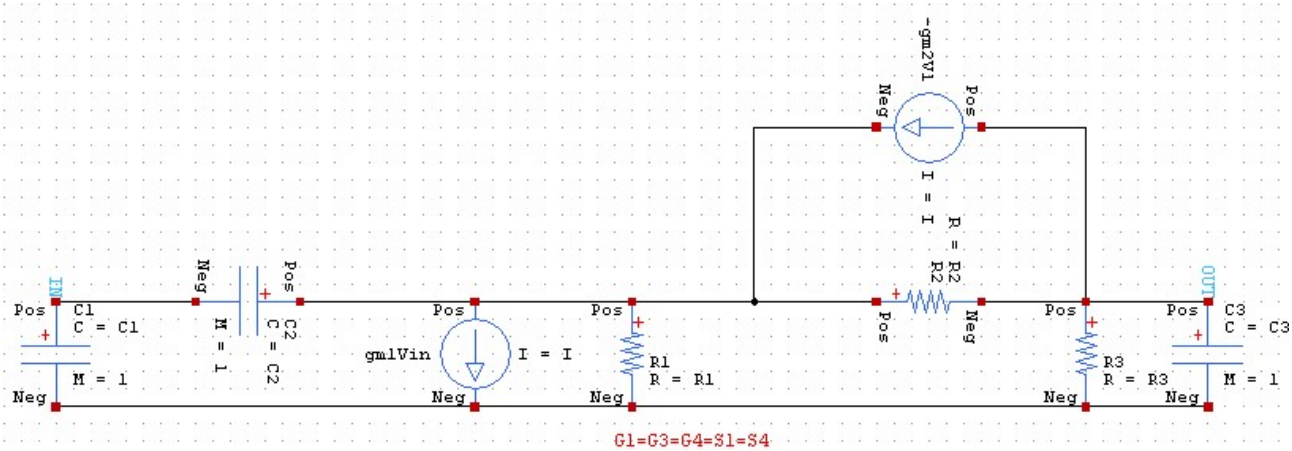


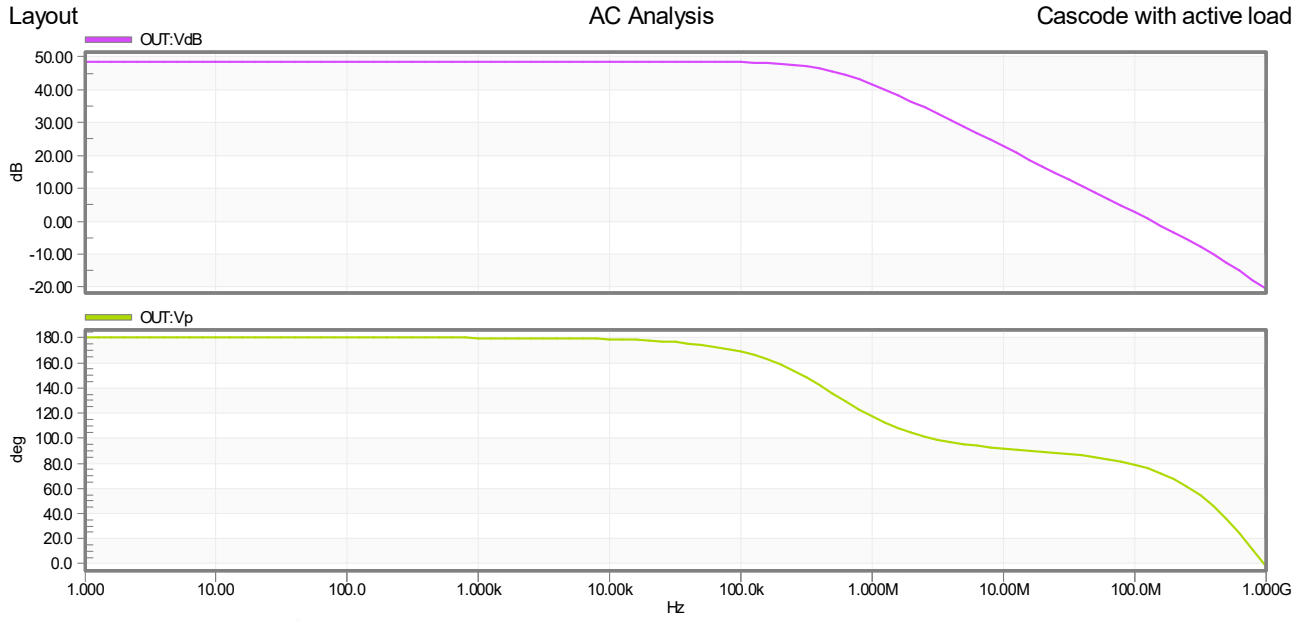
Figure 60: Equivalent circuit of cascode with active load.

AC SMALL-SIGNAL MODELS: temperature=25.0

	0	1	2	3
	M1	M2	M3	M4
MODEL	MODN	MODN	MODP	MODP
TYPE	NMOS	NMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	30.0021u	30.0021u	-30.0021u	30.0000u
IBS	0.	-2.2036f	0.	1.7015f
IBD	-2.2036f	-8.4920f	1.7034f	0.
VGS	604.8412m	767.2333m	-963.3126m	0.
VDS	606.0667m	1.7296	-964.3674m	963.3126m
VBS	0.	-606.0667m	0.	963.3126m
VTH	558.2320m	724.8964m	-756.8839m	-756.8840m
VDSAT	94.6272m	95.9282m	-218.1933m	-218.1932m
BETA	9.6110m	9.5483m	1.2680m	1.2680m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	525.2004u	535.1937u	247.1152u	-247.0998u
GDS	1.6991u	662.3123n	1.9641u	-1.9650u
GMB	163.4315u	128.1891u	53.4409u	-53.4375u
GBD	3.6359f	3.6359f	1.7663f	1.7663f
GBS	3.6359f	3.6359f	1.7663f	1.7663f
CDTOT	56.9474f	49.2571f	47.0418f	126.3712f
CGTOT	84.6195f	82.6358f	140.5854f	140.5856f
CSTOT	96.0094f	87.2377f	126.3711f	47.0520f
CBTOT	125.4009f	105.1100f	122.1225f	122.1326f
CGS	63.0104f	63.0030f	122.6341f	9.5237f
CGD	10.8679f	10.8575f	9.5237f	122.6342f
CGB	10.7413f	8.7752f	8.4277f	8.4277f
CBD	46.0677f	38.3832f	37.5191f	52.7129f
CBS	52.6422f	46.0677f	52.7129f	37.5292f

Figure 61: Small signal parameters of cascode with active load.

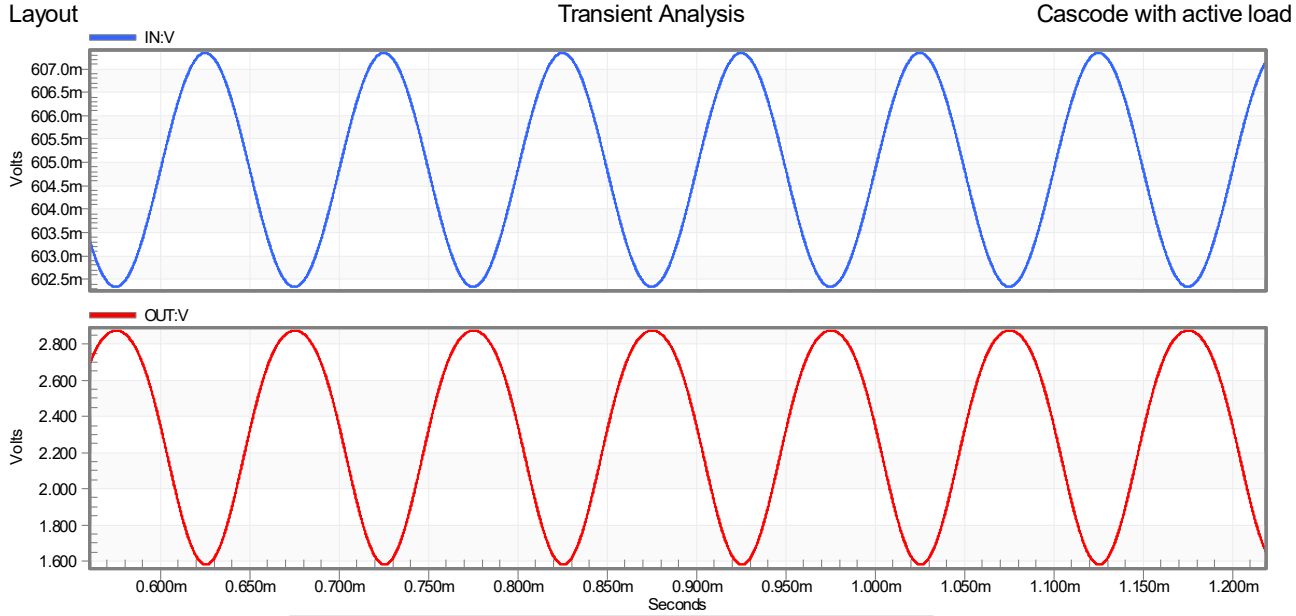
Figure 62 shows the AC analysis of cascode with cascode load. The circuit has a maximum gain around 48dB or Av=265. The unity gain bandwidth (ft) of the amplifier is around 137Mhz and this can be found when the characteristic of gain reaches 0dB. At 0dB the unity gain bandwidth frequency provides us information about the phase margin (PM). Because the phase margin is above 45° this means that the system is stable and in the output response we have no ringing. The bandwidth of the amplifier is determined by the -3dB which is the dominant pole at frequency of 514kHz as shown in (Fig. 62). The theoretical calculations using MATLAB (code 21) based on (Netlist 11) are in close agreement (Fig. 62).




```
Measurement result summary
   Av_dB                =   48.5137
   PM                   =   74.6296
   ft                   =  137.1917MEG
   minus_threedb_pole   =  513.7685k
```

Figure 62: AC analysis of cascode with active load.

Figure 63 shows the transient analysis of cascode with active load. By looking the trace voltage of transient analysis (Fig. 63) we see that the input signal is amplified as many times as the gain we extracted before. Table 4 shows the desired and the achieved performance characteristics of the amplifier.



Trace Name	Y1	Y2	Delta
IN:V	602.3m	607.3m	4.9992m
OUT:V	2.9	1.6	-1.2938

Figure 63: Transient analysis of cascode with active load.

Performance Specifications	Desired Values	Simulation Values
Overall Gain (A_V) (dB)	40	48
Unity Gain Bandwidth (GBW) (Mhz)	≥140	137
Phase Margin (PM) (°)	≥60	74
Output Voltage Swing (V)	0.2-3.1	0.190-3.1

Table 4: Performance results of cascode with active load.

3.4 Cascode with Cascode Load

A viable way to raise the gain would be to increase the aspect ratio of input transistor. But that it's not always a preferable way. The most common way is to increase the output resistance and try to keep the area as minimum as possible. This can be achieved by having a cascode load and therefore the output resistance is enhanced even more from the cascode with active load. This implementation is very common for single stage amplifiers.

In our case we have the same specifications with inverter with active load. We follow the same design method. To find the bias voltages we use diode connection transistors with a dc current source 30μA and power supply at 3.3V.

Biasing the input transistor M1 at VGS1=604.8412mV, biasing the cascode input transistor M2 at VG2=VDS1+VGS2=1.3733V. Finally using the structure bellow, we can find the biasing voltage of M3=MPtest3. Then VG3=VDD-VDS(MPtest4)-VGS(MPtest3)=1.2037V as shown in (Fig. 66). Figure 66 shows the schematic design of cascode with cascode load and Fig. 67 shows its layout.

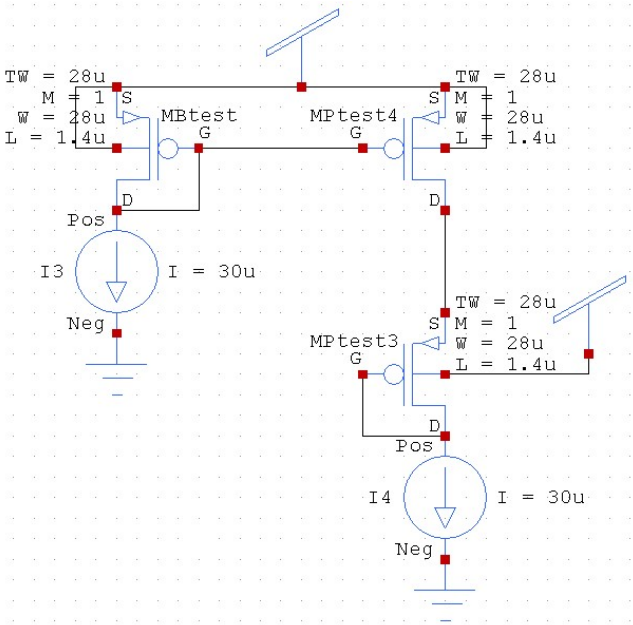


Figure 64: Biasing configuration for the cascode load.

	8	9	10
	MMBtest	MMPtest3	MMPtest4
MODEL	MODP	MODP	MODP
TYPE	PMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation
ID	-30.0000u	-30.0000u	-30.0000u
IBS	0.	1.7015f	0.
IBD	1.7015f	3.7027f	1.7015f
VGS	-963.3126m	-1.1330	-963.3126m
VDS	-963.3126m	-1.1330	-963.3111m
VBS	0.	963.3111m	0.
VTH	-756.8840m	-929.6760m	-756.8840m
VDSAT	-218.1932m	-229.4446m	-218.1932m
BETA	1.2680m	1.2118m	1.2680m
RS	0.	0.	0.
RD	0.	0.	0.
GM	247.0998u	248.1276u	247.0998u
GDS	1.9650u	1.7725u	1.9650u
GMB	53.4375u	37.2396u	53.4375u
GBD	1.7663f	1.7663f	1.7663f
GBS	1.7663f	1.7663f	1.7663f
CDTOT	47.0520f	39.4267f	47.0520f
CGTOT	140.5856f	137.9404f	140.5856f
CSTOT	126.3712f	107.3566f	126.3712f
CBTOT	122.1326f	89.4355f	122.1326f
CGS	122.6342f	122.1186f	122.6342f
CGD	9.5237f	9.5166f	9.5237f
CGB	8.4277f	6.3052f	8.4277f
CBD	37.5292f	29.9093f	37.5292f
CBS	52.7129f	37.5292f	52.7129f

Figure 65: Small signal parameters for the cascode load.

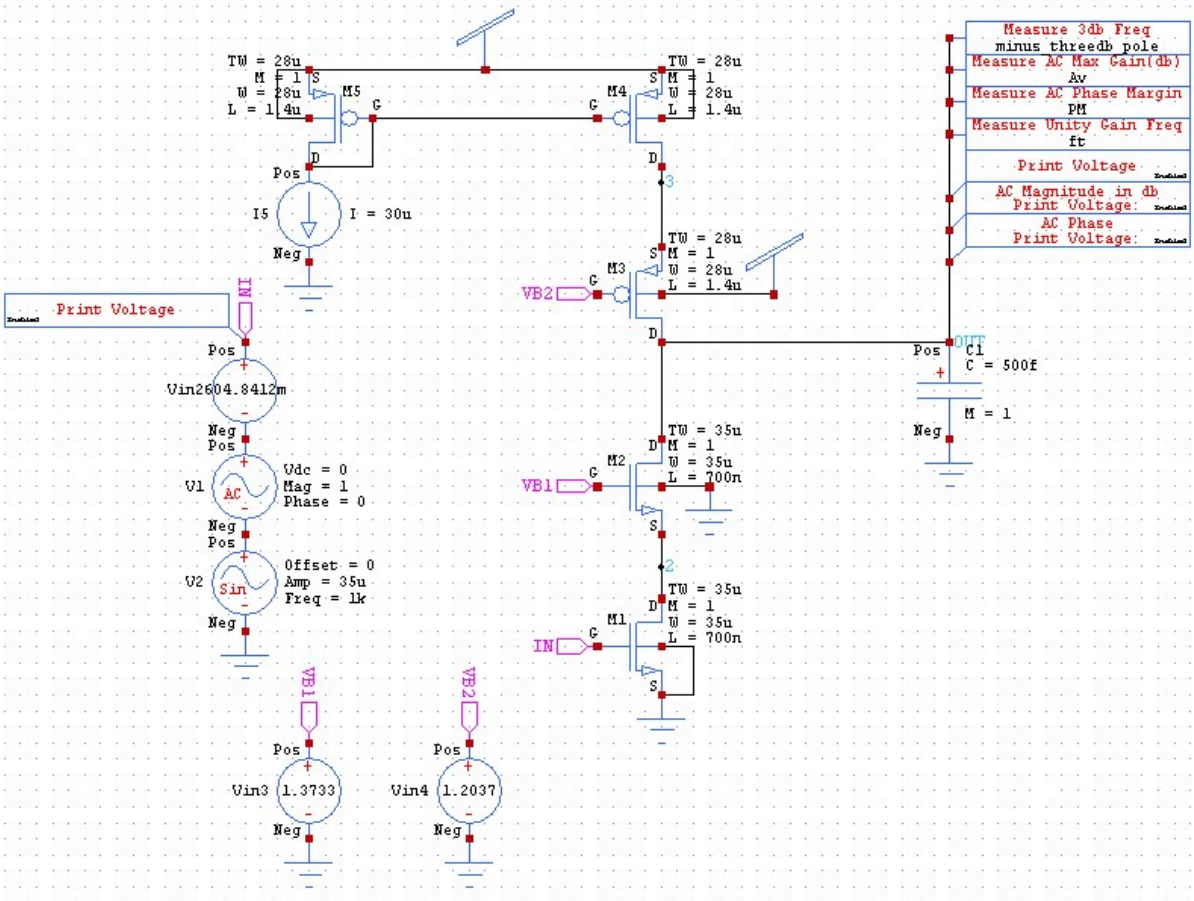


Figure 66: Schematic design of cascode with cascode load.

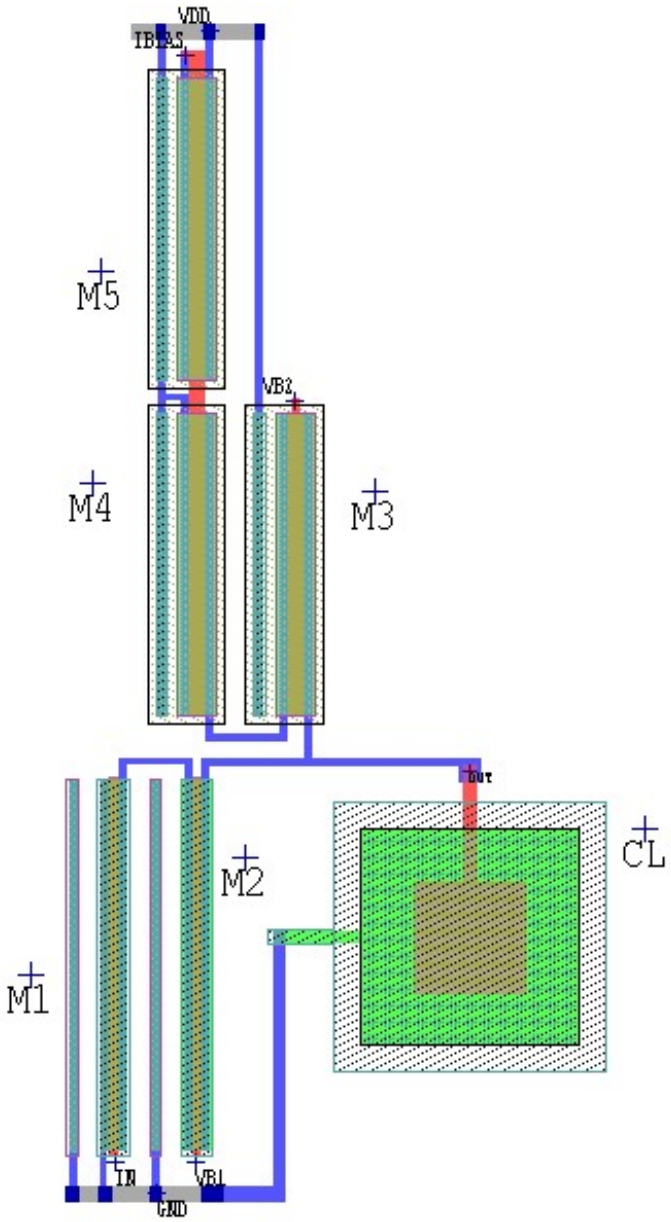


Figure 67: Layout design of cascode with cascode load.

Figure 68 show the equivalent circuit of cascode with cascode load. The small signal parameters that we see on the circuit are calculated on APPENDIX A with code 22 using the small signal parameters of (Fig. 69).

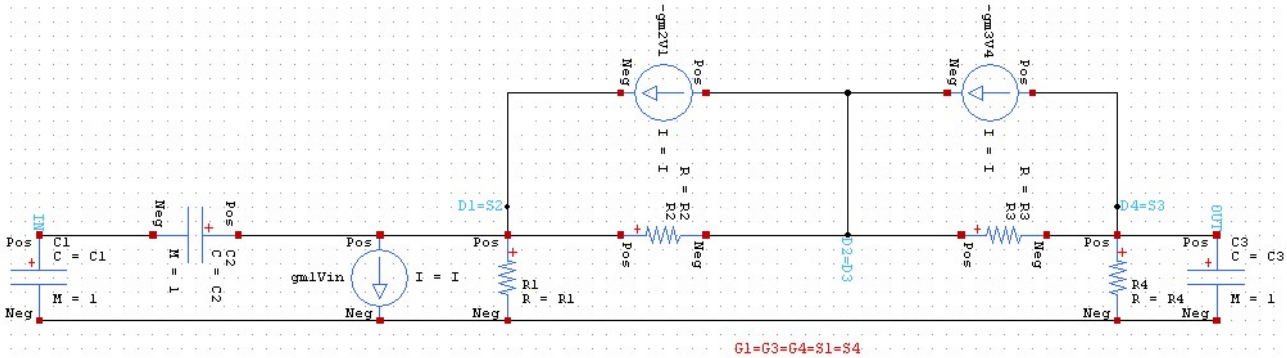


Figure 68: Equivalent circuit of cascode with cascode load.

AC SMALL-SIGNAL MODELS: temperature=25.0

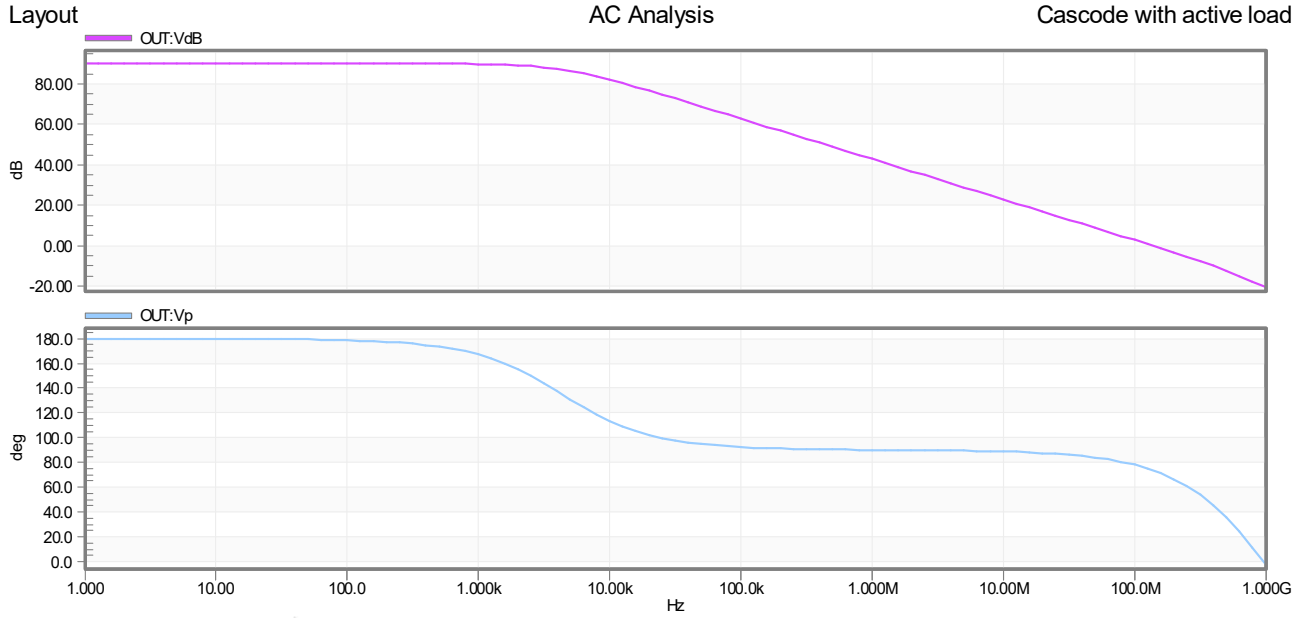
	0	1	2	3
	M1	M2	M3	M4
MODEL	MODN	MODN	MODP	MODP
TYPE	NMOS	NMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	29.9995u	29.9995u	-29.9995u	30.0000u
IBS	0.	-2.1981f	0.	1.7015f
IBD	-2.1981f	-4.5355f	1.7011f	0.
VGS	604.8412m	768.7332m	-963.3126m	0.
VDS	604.5668m	642.8585m	-963.0660m	963.3126m
VBS	0.	-604.5668m	0.	963.3126m
VTH	558.2335m	725.5544m	-756.8841m	-756.8840m
VDSAT	94.6264m	96.4098m	-218.1932m	-218.1932m
BETA	9.6110m	9.5474m	1.2680m	1.2680m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	525.1546u	532.6640u	247.0962u	-247.0998u
GDS	1.7047u	1.5884u	1.9652u	-1.9650u
GMB	163.4174u	127.6474u	53.4367u	-53.4375u
GBD	3.6359f	3.6359f	1.7663f	1.7663f
GBS	3.6359f	3.6359f	1.7663f	1.7663f
CDTOT	56.9589f	53.1255f	47.0543f	126.3712f
CGTOT	84.6194f	82.8981f	140.5856f	140.5856f
CSTOT	96.0093f	87.4407f	126.3712f	47.0520f
CBTOT	125.4124f	109.0063f	122.1350f	122.1326f
CGS	63.0101f	63.3188f	122.6342f	9.5237f
CGD	10.8679f	10.8637f	9.5237f	122.6342f
CGB	10.7414f	8.7156f	8.4277f	8.4277f
CBD	46.0791f	42.2471f	37.5316f	52.7129f
CBS	52.6422f	46.0791f	52.7129f	37.5292f

	4
	M5
MODEL	MODP
TYPE	PMOS
REGION	Saturation
ID	-29.9995u
IBS	1.7011f
IBD	3.6255f
VGS	-1.1332
VDS	-1.0895
VBS	963.0660m
VTH	-929.6439m
VDSAT	-229.7102m
BETA	1.2118m
RS	0.
RD	0.
GM	247.8900u
GDS	1.8028u
GMB	37.2044u
GBD	1.7663f
GBS	1.7663f
CDTOT	39.6395f
CGTOT	137.9465f
CSTOT	107.3625f
CBTOT	89.6507f
CGS	122.1239f
CGD	9.5183f
CGB	6.3042f
CBD	30.1210f
CBS	37.5316f

Figure 69: Small signal parameters of cascode with cascode load.

Figure 70 shows the AC analysis of cascode with cascode load. The circuit has a maximum gain around 90dB or Av=32000. The unity gain bandwidth (ft) of the amplifier is around 138Mhz and this can be found when the characteristic of gain reaches 0dB. At 0dB the bandwidth frequency provides us information about the phase margin (PM). Because the phase margin is above 45° this means that the system is stable and in the output response we have no ringing. The bandwidth of the amplifier is determined by the -3dB which is the dominant pole

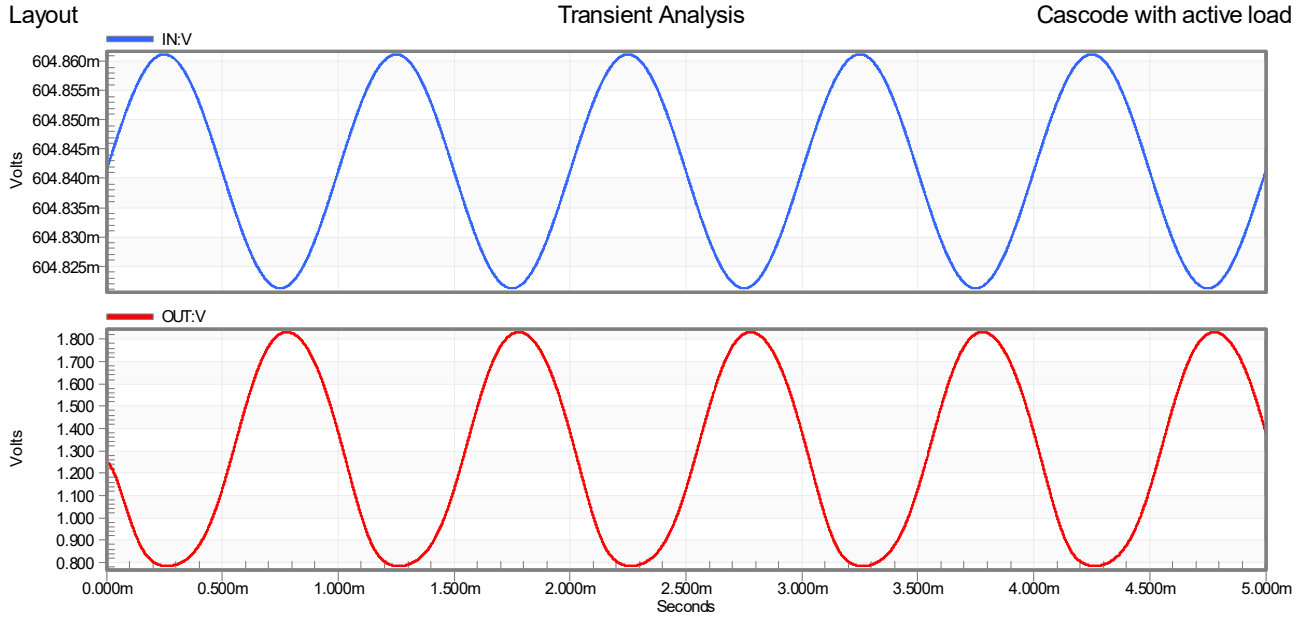
at frequency of 4.3kHz as shown in (Fig. 70). The theoretical calculations using MATLAB (code 22) based on (Netlist 12) are in close agreement (Fig. 70).




```
Measurement result summary
   Av_dB                =   90.1147
   PM                   =   73.6763
   ft                   =  138.6606MEG
   minus_threedb_pole =    4.3537k
```

Figure 70: AC analysis of cascode with cascode load.

Figure 71 shows the transient analysis of cascode with cascode load. By looking the trace voltage of transient analysis (Fig. 71) we see that the input signal is amplified as many times as the gain we extracted before. Table 5 shows the desired and the achieved performance characteristics of the amplifier.



Trace Name	Y1	Y2	Delta
IN:V	604.8m	604.9m	39.6126u
OUT:V	1.8	784.0m	-1.0478

Figure 71: Transient analysis of cascode with cascode load.

Performance Specifications	Desired Values	Simulation Values
Overall Gain (A_V) (dB)	40	90
Unity Gain Bandwidth (GBW) (Mhz)	≥140	138
Phase Margin (PM) (°)	≥60	73
Output Voltage Swing (V)	0.2-3.1	0.191-2.8

Table 5: Performance results of cascode with cascode load.

3.5 Differential Amplifier

The differential pair is known as the input stage of operational amplifier. It is made from two identical CMOS transistors with their source in common. In our case we use a transistor as current sink. At table 6 we see the performance specifications to design the differential amplifier.

Performance Specifications	Desired Values
VDD (V)	3.3
Overall Gain (A_V) (dB)	40
Unity Gain Bandwidth (GBW) (Mhz)	≥100
-3dB frequency (Khz)	600
Phase Margin (PM) (°)	≥60
CMRR (dB)	≥60
Power Dissipation (P_{diss}) (mW)	0.2
Slew Rate (V/μs)	20
Load Capacitance (C_L) (pF)	0.5

Table 6: Differential amplifier specifications.

For $f_{-3dB} \rightarrow R_{out} = \frac{gds4}{gds5} = \frac{1}{2\pi \cdot 600 \cdot 10^3 \cdot 0.5 \cdot 10^{-12}} = 530kohms$

Using for input transistor minimum length $L_n = 0.7\mu m$ and for the load of differential $L_p = 1.4\mu m$. To meet the slew rate $I_{bias,min} = \frac{20}{10^{-6}} \cdot 0.5 \cdot 10^{-12} = 10\mu A$. For maximum current $I_{bias,max} = \frac{0.2mW}{3.3V} = 60\mu A$.

We use the maximum current of $I_{bias} = 60\mu A$ for biasing the circuit. So $I_3 = 60\mu A$. The current in differential pair will be $I_2 = I_4 = 30\mu A$.

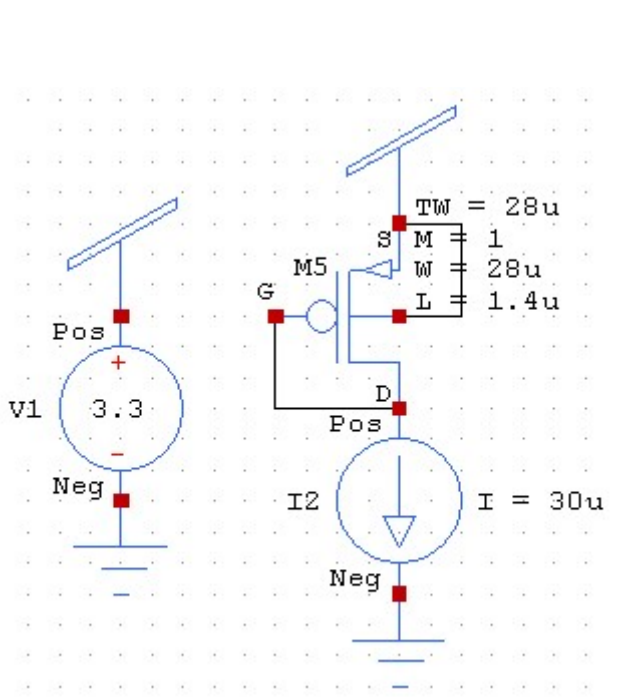
To meet $R_{out} = 530kohms$ remembering that $\frac{w}{L} = \frac{28\mu m}{1.4\mu m}$ gives us a resistor near to 530kohms then using a diode configuration for M5 and M6 by biasing with 30μA current we have $gds5 = 1.9650\mu S$. Keeping the load in that dimension we can achieve the f_{-3dB}.

Using the same aspect ratio with the above circuits M2 and M4 $\frac{w}{L} = \frac{35\mu m}{0.7\mu m}$ to achieve a high gain and enough bandwidth as shown in (Fig. 74).

The biasing transistor M3 and M1 using same length as the input transistor, we enlarge the width in order to achieve the minimum output swing for our common mode as shown in (Fig. 73).

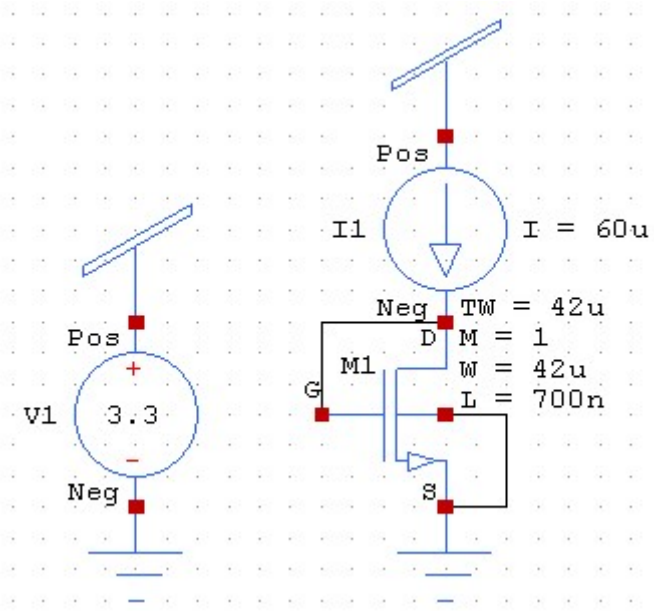
Finally the dc biasing for transistors M2 and M4: VG1=VG2=VDS3+VGS4=1.239V.

Figure 75 shows the schematic design of differential amplifier and Fig. 76 shows its layout. The small signal results of the differential amplifier are shown in Fig. 77.



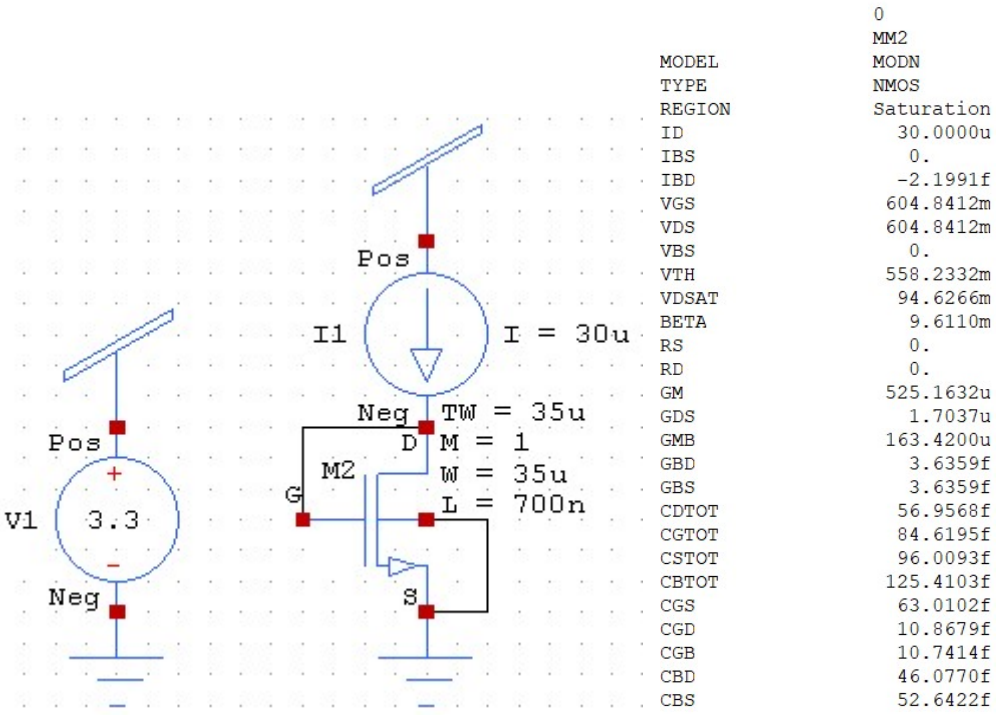
	0
	MM5
MODEL	MODP
TYPE	PMOS
REGION	Saturation
ID	-30.0000u
IBS	0.
IBD	1.7015f
VGS	-963.3126m
VDS	-963.3126m
VBS	0.
VTH	-756.8840m
VDSAT	-218.1932m
BETA	1.2680m
RS	0.
RD	0.
GM	247.0998u
GDS	1.9650u
GMB	53.4375u
GBD	1.7663f
GBS	1.7663f
CDTOT	47.0520f
CGTOT	140.5856f
CSTOT	126.3712f
CBTOT	122.1326f
CGS	122.6342f
CGD	9.5237f
CGB	8.4277f
CBD	37.5292f
CBS	52.7129f

Figure 72: Differential load transistor of the differential amplifier.



	0
	MM1
MODEL	MODN
TYPE	NMOS
REGION	Saturation
ID	60.0000u
IBS	0.
IBD	-2.7578f
VGS	634.7291m
VDS	634.7291m
VBS	0.
VTH	557.2672m
VDSAT	113.4805m
BETA	11.5354m
RS	0.
RD	0.
GM	926.0000u
GDS	3.2311u
GMB	287.2264u
GBD	4.3449f
GBS	4.3449f
CDTOT	67.9556f
CGTOT	108.1653f
CSTOT	120.5592f
CBTOT	150.3656f
CGS	84.4599f
CGD	13.0296f
CGB	10.6758f
CBD	54.9103f
CBS	63.0511f

Figure 73: Biasing transistor of the differential amplifier.



	0
	MM2
MODEL	MODN
TYPE	NMOS
REGION	Saturation
ID	30.0000u
IBS	0.
IBD	-2.1991f
VGS	604.8412m
VDS	604.8412m
VBS	0.
VTH	558.2332m
VDSAT	94.6266m
BETA	9.6110m
RS	0.
RD	0.
GM	525.1632u
GDS	1.7037u
GMB	163.4200u
GBD	3.6359f
GBS	3.6359f
CDTOT	56.9568f
CGTOT	84.6195f
CSTOT	96.0093f
CBTOT	125.4103f
CGS	63.0102f
CGD	10.8679f
CGB	10.7414f
CBD	46.0770f
CBS	52.6422f

Figure 74: Input transistor of the differential amplifier.

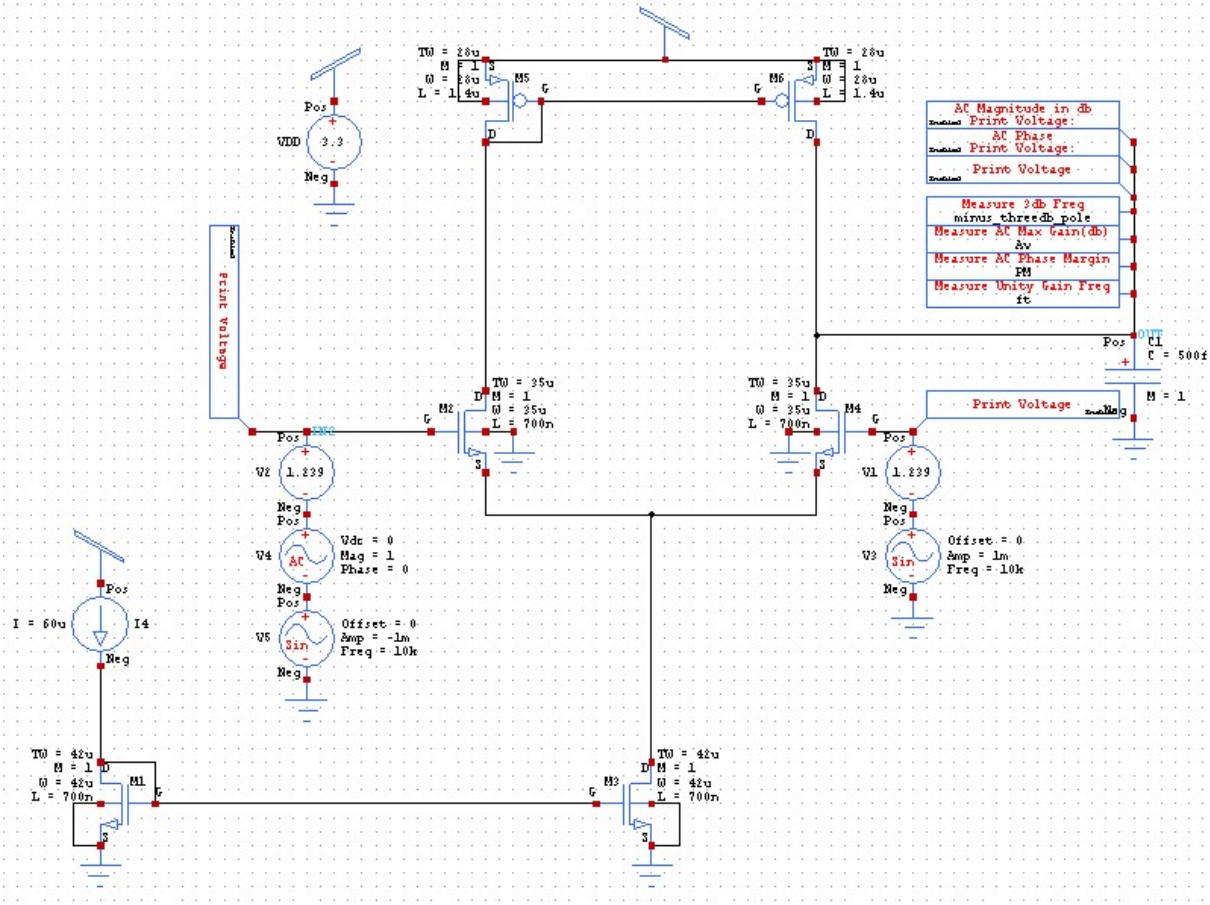


Figure 75: Schematic design of differential amplifier.

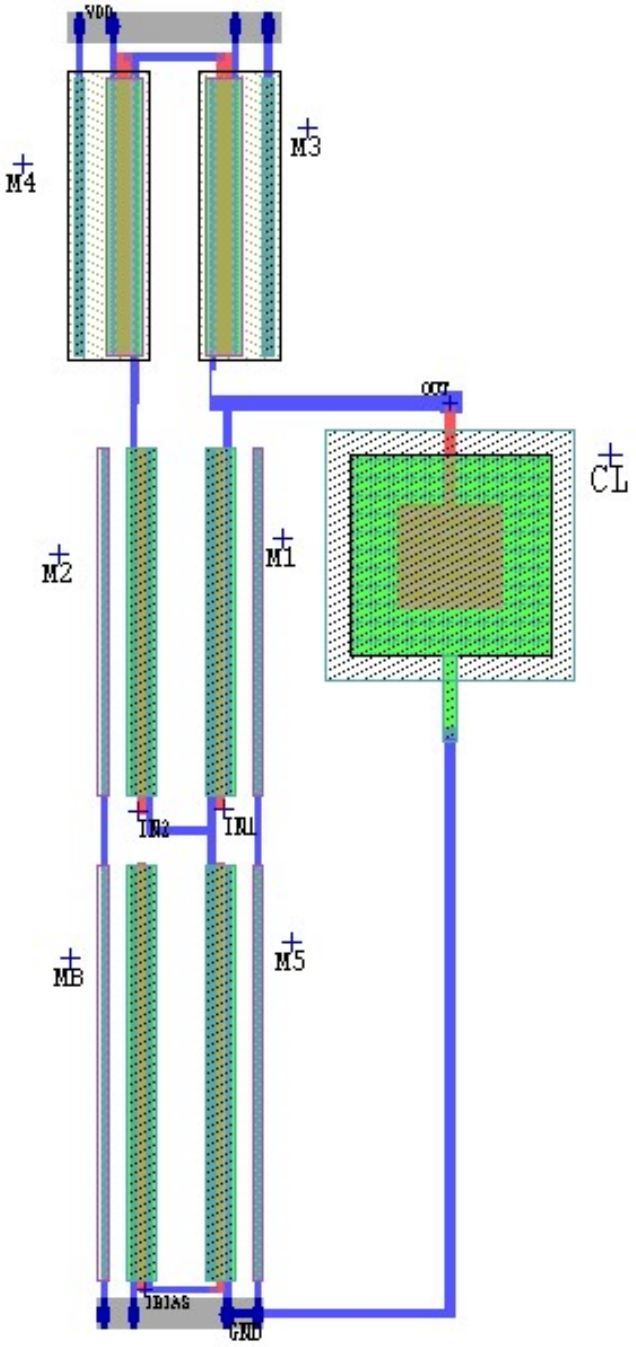


Figure 76: Layout design of differential amplifier.

AC SMALL-SIGNAL MODELS: temperature=25.0

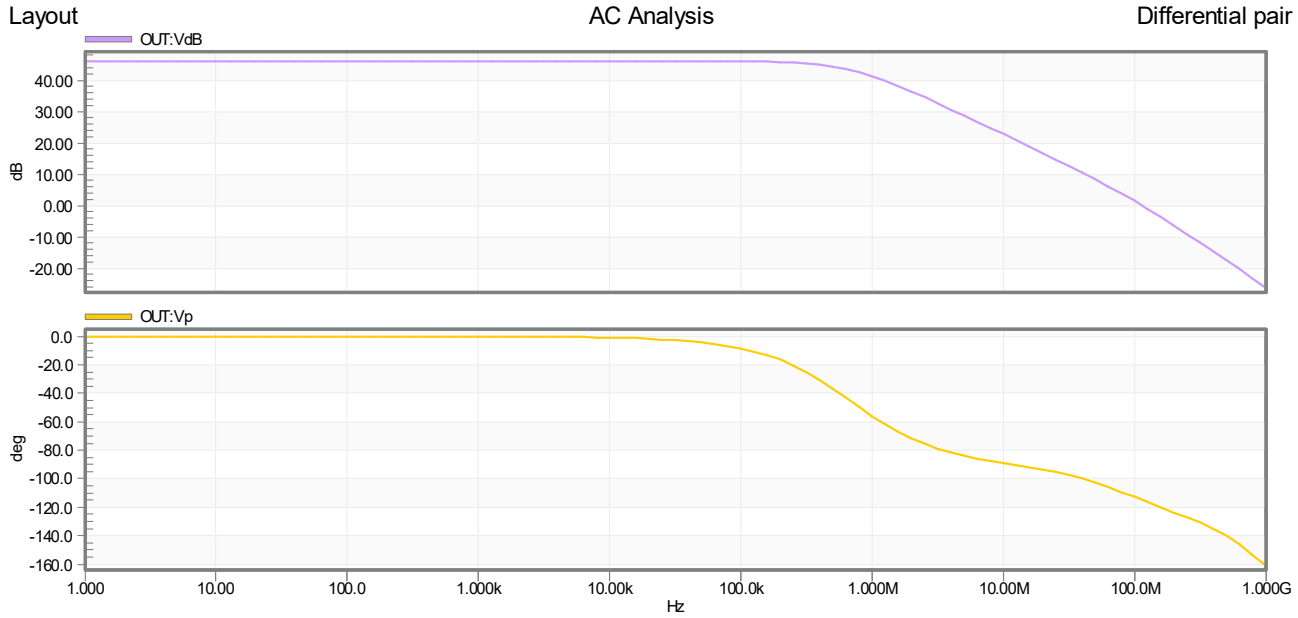
	0	1	2	3
	M1	M2	M3	M4
MODEL	MODN	MODN	MODN	MODN
TYPE	NMOS	NMOS	NMOS	NMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	60.0000u	-29.7376u	-59.4752u	29.7376u
IBS	0.	-8.4997f	-2.1665f	-1.8130f
IBD	-2.7578f	-1.8130f	0.	-8.4997f
VGS	634.7291m	-1.0987	136.0970m	740.3679m
VDS	634.7291m	-1.8391	-498.6321m	1.8391
VBS	0.	-2.3377	-498.6321m	-498.6321m
VTH	557.2672m	698.2196m	557.3963m	698.2196m
VDSAT	113.4805m	95.3764m	113.3967m	95.3764m
BETA	11.5354m	9.5616m	11.5353m	9.5616m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	926.0000u	-530.7612u	-917.3366u	530.7612u
GDS	3.2311u	-640.4055n	-4.6519u	640.4055n
GMB	287.2264u	-132.1806u	-284.5535u	132.1806u
GBD	4.3449f	3.6359f	4.3449f	3.6359f
GBS	4.3449f	3.6359f	4.3449f	3.6359f
CDTOT	67.9556f	88.2325f	120.5699f	49.2514f
CGTOT	108.1653f	82.6894f	108.1843f	82.6894f
CSTOT	120.5592f	49.2514f	69.2605f	88.2325f
CBTOT	150.3656f	106.7271f	151.6640f	106.7271f
CGS	84.4599f	10.8579f	13.0455f	62.7538f
CGD	13.0296f	62.7538f	84.4688f	10.8579f
CGB	10.6758f	9.0778f	10.6701f	9.0778f
CBD	54.9103f	46.9303f	63.0511f	38.3775f
CBS	63.0511f	38.3775f	56.2032f	46.9303f

	4	5
	M5	M6
MODEL	MODP	MODP
TYPE	PMOS	PMOS
REGION	Saturation	Saturation
ID	-29.7376u	29.7376u
IBS	0.	1.6997f
IBD	1.6997f	0.
VGS	-962.2566m	-1.7764f
VDS	-962.2566m	962.2566m
VBS	0.	962.2566m
VTH	-756.8842m	-756.8842m
VDSAT	-217.3186m	-217.3186m
BETA	1.2681m	1.2681m
RS	0.	0.
RD	0.	0.
GM	245.9606u	-245.9606u
GDS	1.9504u	-1.9504u
GMB	53.1930u	-53.1930u
GBD	1.7663f	1.7663f
GBS	1.7663f	1.7663f
CDTOT	47.0620f	126.3655f
CGTOT	140.5779f	140.5779f
CSTOT	126.3655f	47.0620f
CBTOT	122.1475f	122.1475f
CGS	122.6200f	9.5237f
CGD	9.5237f	122.6200f
CGB	8.4343f	8.4343f
CBD	37.5393f	52.7129f
CBS	52.7129f	37.5393f

Figure 77: Small signal parameters of differential amplifier.

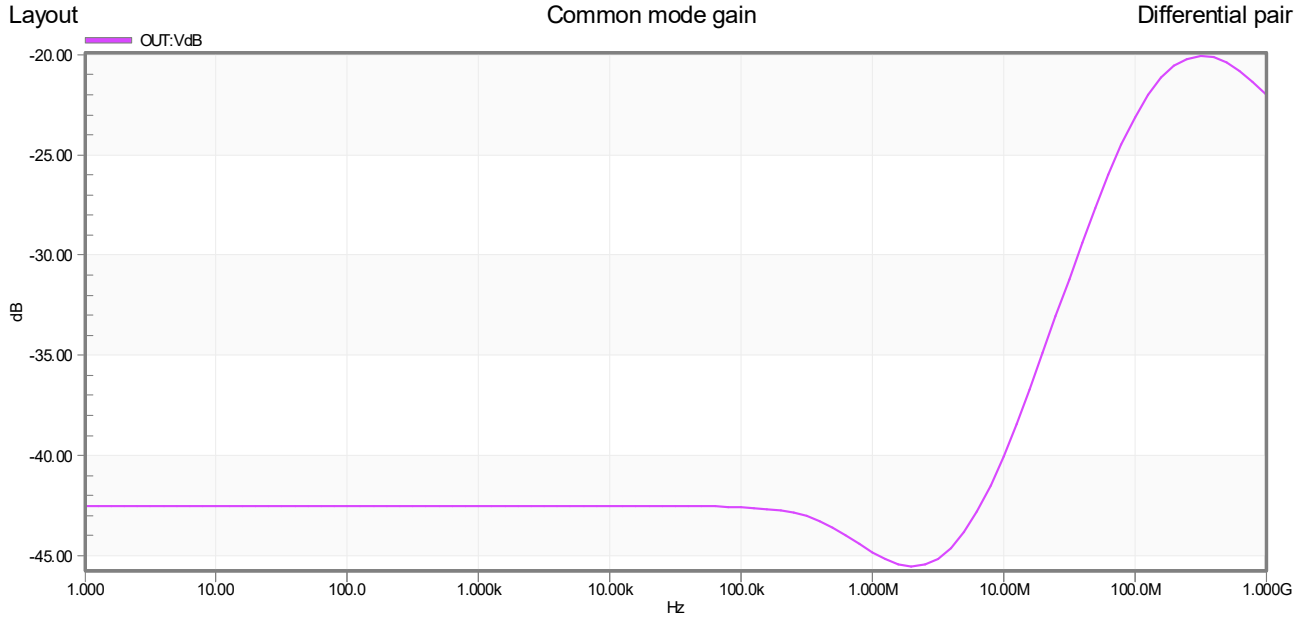
Figure 78 shows the AC analysis of differential amplifier. The circuit has a maximum gain around 46dB or Av=46. The unity gain bandwidth (ft) of the amplifier is around 115Mhz and this can be found when the characteristic of gain reaches 0dB. At 0dB the unity gain bandwidth frequency provides us information about the phase margin (PM). Because the phase margin is

above 45° this means that the system is stable and in the output response we have no ringing. Also a very important parameter for the differential amplifier is the common mode rejection ratio. By extracting the common mode gain (Fig. 79) we calculated the CMRR around 66dB or Av=2000 which ensures a good ratio between the differential and the common mode gain. CMRR=differential gain-common mode gain=46-(-20)=66dB. The bandwidth of the amplifier is determined by the -3dB which is the dominant pole at frequency of 677kHz as shown in (Fig. 78).




```
Measurement result summary
   Av_dB              =   46.1948
   PM                 = -115.0127
   ft                 =  115.1439MEG
   minus_threedb_pole =  676.9362k
```

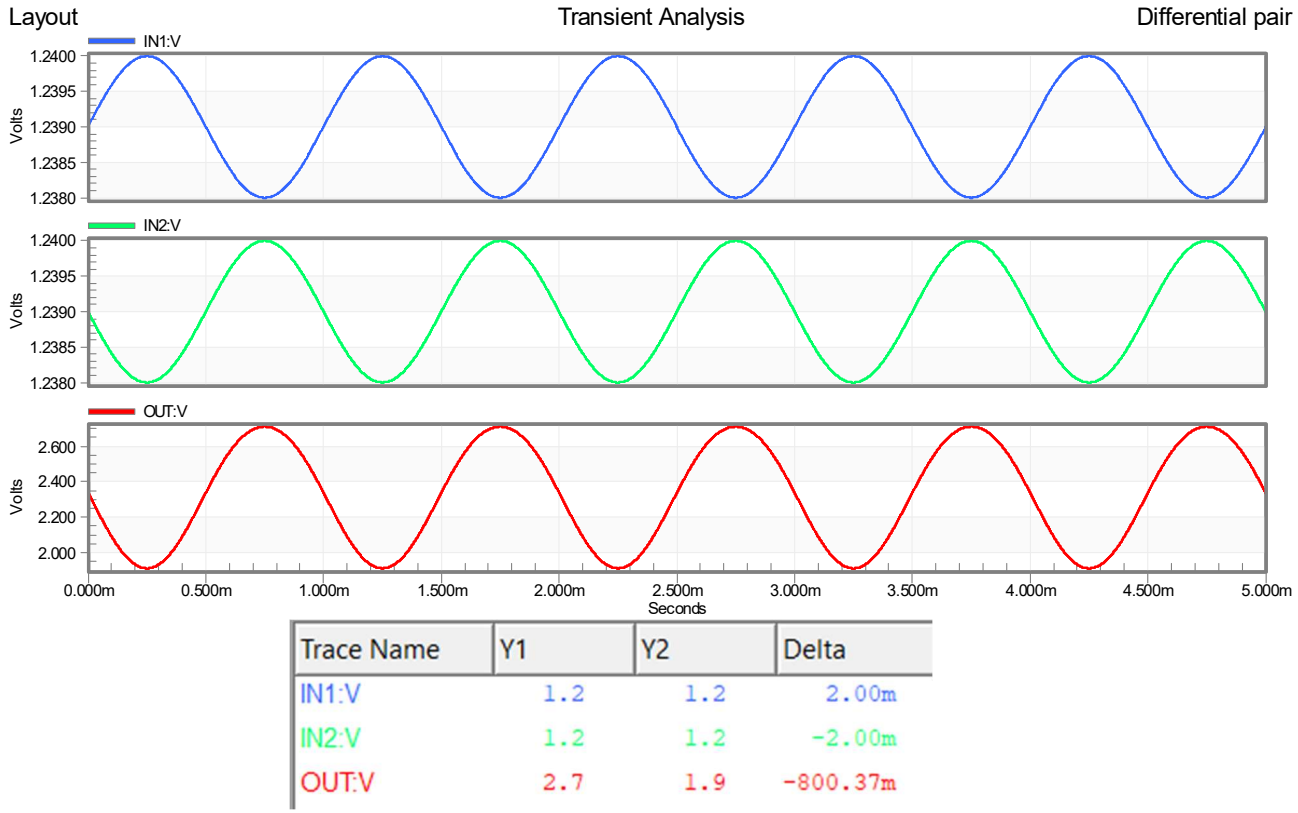
Figure 78: AC analysis of differential amplifier.



```
Measurement result summary
   Av                    =   -20.0644
```

Figure 79: AC analysis of differential amplifier.

Figure 80 shows the transient analysis of differential amplifier. By looking the trace voltage of transient analysis (Fig. 80) we see that the input signal is amplified as many times as the gain we extracted before. Figure 81 shows the power dissipation of the differential amplifier around 0.39mW. Table 7 shows the desired and the achieved performance characteristics of the amplifier.



Trace Name	Y1	Y2	Delta
IN1:V	1.2	1.2	2.00m
IN2:V	1.2	1.2	-2.00m
OUT:V	2.7	1.9	-800.37m

Figure 80: Transient analysis of differential amplifier.

```
Average power consumed -> 3.942679e-04 watts
```

Figure 81: Power dissipation of differential amplifier.

Performance Specifications	Desired Values	Simulation Values
Overall Gain (A_V) (dB)	40	46
Unity Gain Bandwidth (GBW) (Mhz)	≥100	115
Phase Margin (PM) (°)	≥60	65
CMRR (dB)	≥60	66
-3dB frequency (kHz)	600	676
Power Dissipation (P_{diss}) (mW)	0.2	0.4

Table 7: Performance results of differential amplifier.

4 CMOS Operational Amplifiers

4.1 Single Stage Mirrored Cascode OTA

Performance Specifications	Desired Values
VDD (V)	3.3
Overall Gain (A_V) (dB)	80
Unity Gain Bandwidth (GBW) (Mhz)	≥50
Phase Margin (PM) (°)	≥50
Power Dissipation (P_{diss}) (mW)	1

Table 8: Single stage mirrored cascode OTA specifications.

At table 8 we see the performance specifications. Based on this we continue with the following design method.

Finding the maximum available current for the circuit $I_{bias} = \frac{1m}{3.3V} = 300\mu A$. Assuming that the mirror factor pair M9-M10 and M11-M12 is 1:1 the bias current is equally distributed between this four transistors. The current in the output branches is 75μA. The tail current that crosses M4 of the differential pair is 150μA. For the input pair (Fig. 82) of differential $g_m = 1.0194mA/V$ which is enough for achieving the 80dB gain. SPICE result are shown in (Fig. 83). With that transconductance the output resistance must be approximately 10Mohms to achieve the gain. SPICE results for the output resistance are shown in (Fig. 84). From the cascode with cascode load circuit we use the same aspect ratio for the load of the upper cascode branch. We change the length of the transistor that looks on the output node in order to achieve a lower output conductance and hence to have a higher resistance. To keep it symmetric we follow the same idea for the lower cascode. With MATLAB calculations (code 23) based on SPICE results (Fig. 84) we have an output resistance of 12Mohms. Finally the schematic design is shown in (Fig. 86) and Fig. 87 shows its layout. The SPICE small signal parameters of the single stage mirrored cascode OTA are shown in (Fig. 88). On APPENDIX B we can study the Netlist of the circuit (Netlist 14).

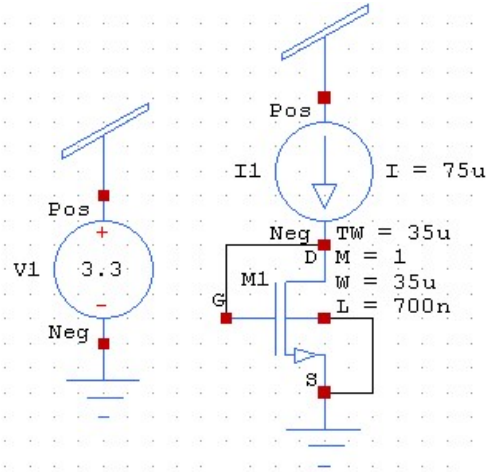


Figure 82: Input transistor of differential pair.

	0
	MM1
MODEL	MODN
TYPE	NMOS
REGION	Saturation
ID	75.0000u
IBS	0.
IBD	-2.4128f
VGS	663.6130m
VDS	663.6130m
VBS	0.
VTH	558.1774m
VDSAT	132.3482m
BETA	9.6006m
RS	0.
RD	0.
GM	1.0194m
GDS	3.8465u
GMB	315.7852u
GBD	3.6359f
GBS	3.6359f
CDTOT	56.5192f
CGTOT	92.9880f
CSTOT	102.8721f
CBTOT	125.4326f
CGS	74.1574f
CGD	10.8659f
CGB	7.9648f
CBD	45.6398f
CBS	52.6422f

Figure 83: Small signal results of the input transistor.

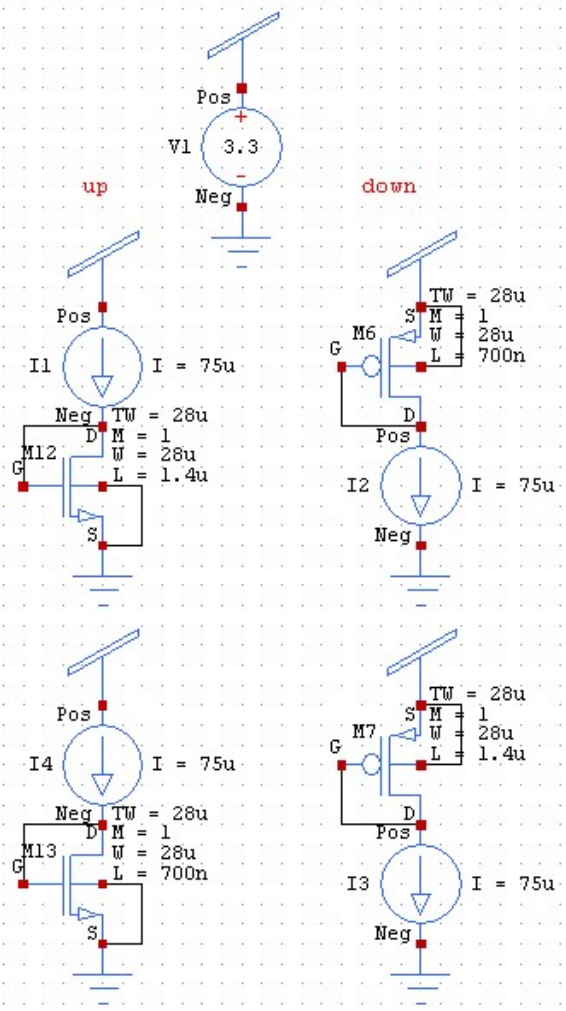


Figure 84: Upper and lower cascode transistor branches.

	0	1	2	3
	MM12	MM13	MM6	MM7
MODEL	MODN	MODN	MODP	MODP
TYPE	NMOS	NMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	75.0000u	75.0000u	-75.0000u	-75.0000u
IBS	0.	0.	0.	0.
IBD	-2.1353f	-1.9960f	1.7416f	1.9488f
VGS	729.5724m	681.9728m	-986.0026m	-1.1033
VDS	729.5724m	681.9728m	-986.0026m	-1.1033
VBS	0.	0.	0.	0.
VTH	528.1042m	559.3474m	-766.7757m	-756.8685m
VDSAT	193.7476m	144.4755m	-237.6279m	-336.2782m
BETA	3.6915m	7.6694m	2.6579m	1.2479m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	673.4910u	939.8841u	571.7416u	386.0627u
GDS	2.6893u	3.7346u	9.4612u	4.2435u
GMB	207.0612u	291.1138u	119.4486u	83.1590u
GBD	2.9268f	2.9268f	1.7663f	1.7663f
GBS	2.9268f	2.9268f	1.7663f	1.7663f
CDTOT	45.0127f	45.2311f	46.7731f	45.7878f
CGTOT	145.4628f	75.2770f	74.3636f	140.7711f
CSTOT	122.9065f	83.1104f	90.8135f	126.5529f
CBTOT	125.0869f	100.5138f	104.2610f	120.2194f
CGS	125.3860f	60.4816f	60.7776f	123.5119f
CGD	8.7725f	8.7025f	9.4122f	9.5321f
CGB	11.3044f	6.0930f	4.1739f	7.7271f
CBD	36.2514f	36.5178f	37.3141f	36.2590f
CBS	42.2333f	42.2333f	52.7129f	52.7129f

Figure 85: Small signal results of upper and lower cascode branches.

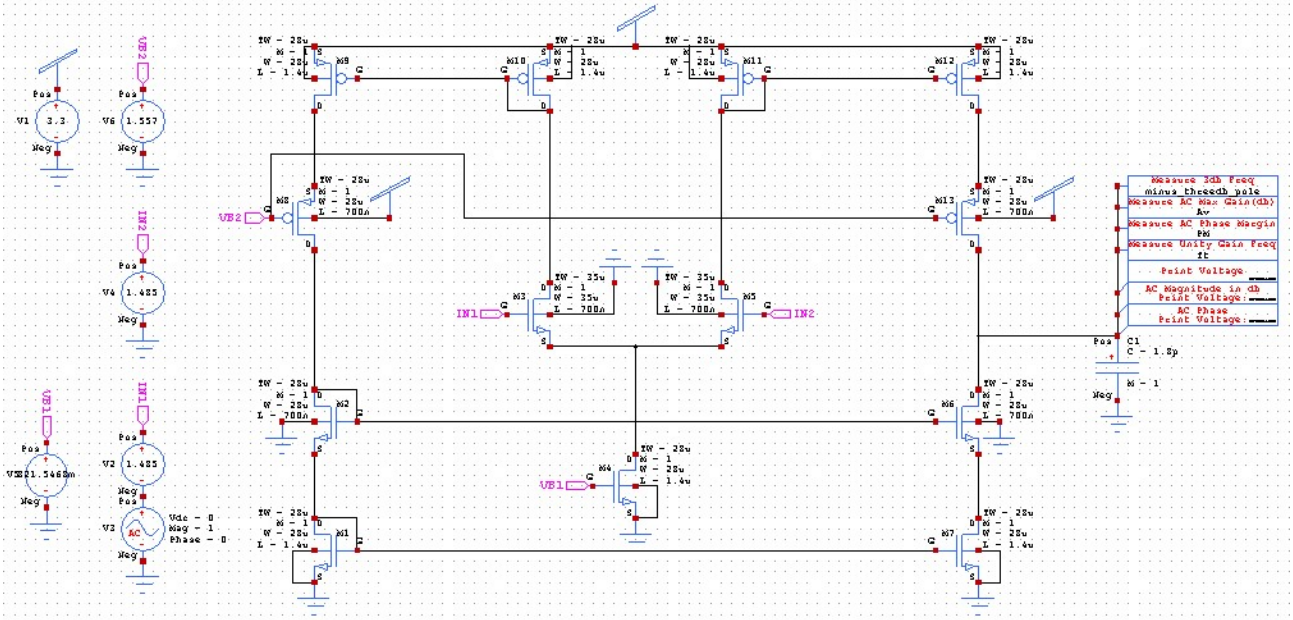


Figure 86: Schematic design of single stage mirrored cascode OTA.

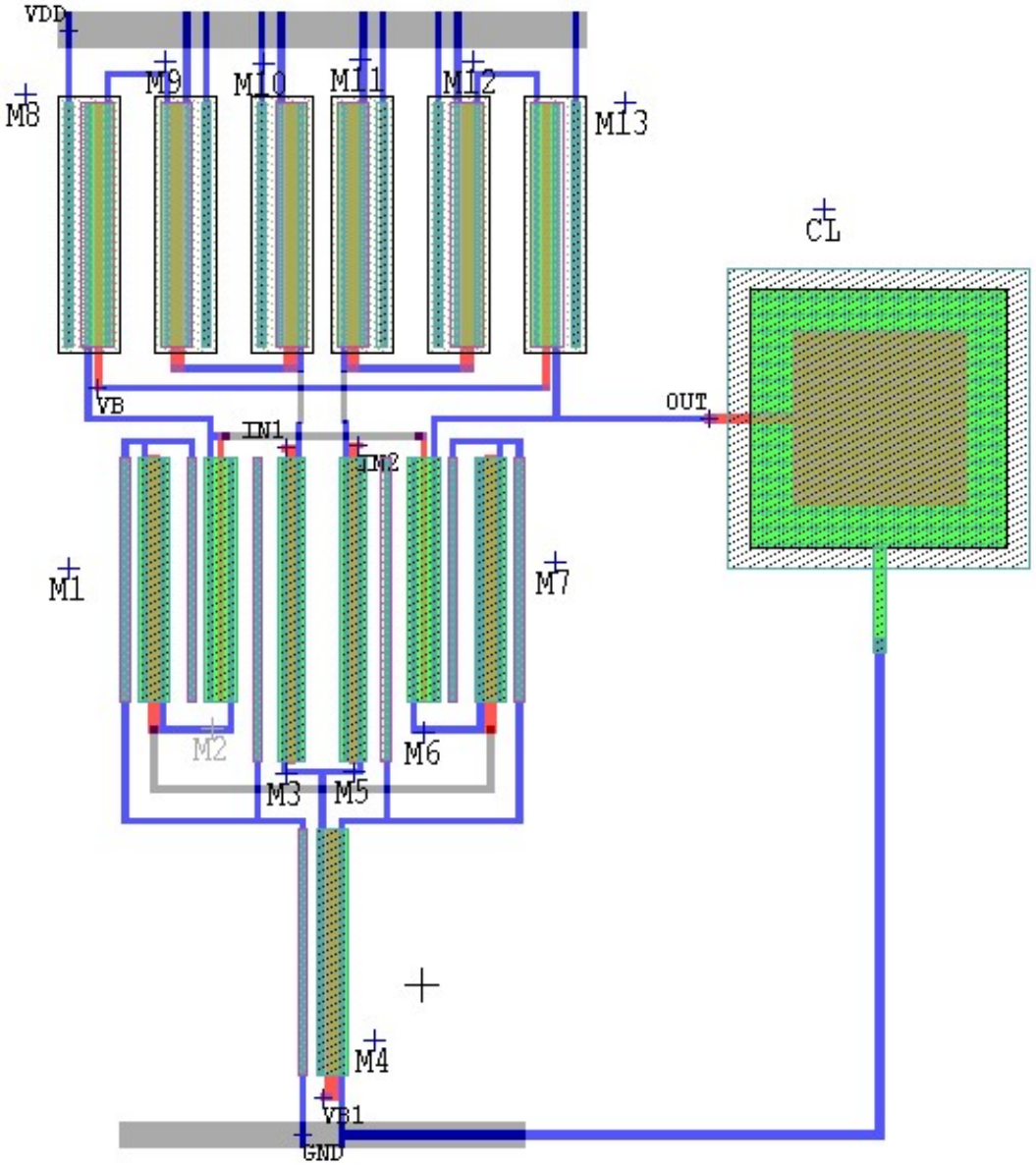


Figure 87: Layout design of single stage mirrored cascode OTA.

	0	1	2	3
	M1	M2	M3	M4
MODEL	MODN	MODN	MODN	MODN
TYPE	NMOS	NMOS	NMOS	NMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	72.2288u	-72.2288u	74.5161u	-149.0345u
IBS	0.	-4.7377f	-2.3617f	-1.9011f
IBD	-2.1232f	-2.1539f	-7.9914f	0.
VGS	725.4337m	0.	835.4547m	172.0015m
VDS	725.4337m	-870.2651m	1.5484	-649.5453m
VBS	0.	-1.5957	-649.5453m	-649.5453m
VTH	528.1042m	755.2798m	735.5209m	528.1042m
VDSAT	190.5888m	144.9468m	133.7755m	263.7795m
BETA	3.6920m	7.5955m	9.5229m	3.6810m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	660.3680u	-922.0275u	1.0257m	-936.6558u
GDS	2.6106u	-2.5388u	1.4881u	-6.9139u
GMB	203.0499u	-211.8063u	241.5739u	-287.2854u
GBD	2.9268f	2.9691f	3.6359f	2.9268f
GBS	2.9268f	2.9691f	3.6359f	2.9268f
CDTOT	45.0350f	82.4154f	49.6378f	123.2215f
CGTOT	145.4214f	74.4875f	92.0476f	145.8386f
CSTOT	122.8706f	47.7620f	93.6020f	45.5368f
CBTOT	125.1280f	98.8664f	105.1545f	125.1153f
CGS	125.3106f	8.6925f	74.8127f	8.8647f
CGD	8.7718f	60.9734f	10.8491f	126.2677f
CGB	11.3390f	4.8217f	6.3858f	10.7062f
CBD	36.2741f	43.6570f	38.7685f	42.2333f
CBS	42.2333f	39.0541f	45.7424f	36.7057f

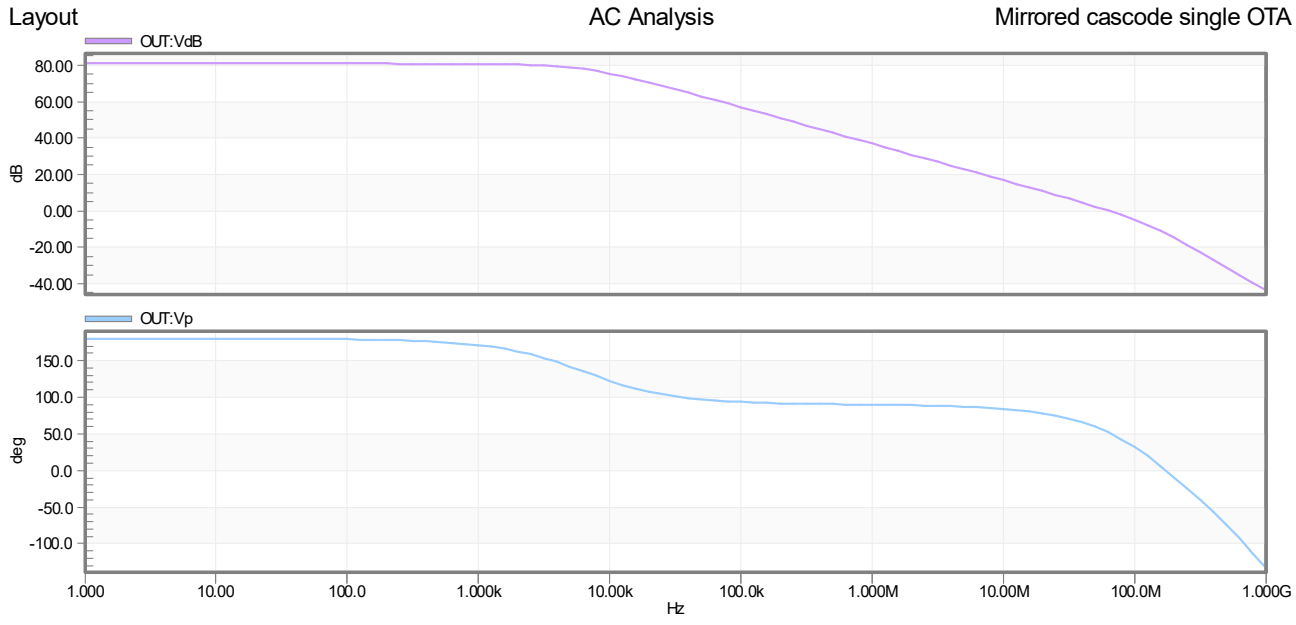
	4	5	6	7
	M5	M6	M7	M8
MODEL	MODN	MODN	MODN	MODP
TYPE	NMOS	NMOS	NMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	-74.5184u	72.2289u	-72.2289u	72.2288u
IBS	-7.9916f	-2.1540f	-2.1234f	3.0817f
IBD	-2.3617f	-4.8112f	0.	1.1692f
VGS	-712.9384m	870.2110m	-54.1035u	-38.6988m
VDS	-1.5484	894.9472m	-725.4878m	1.0577
VBS	-2.1979	-725.4878m	-725.4878m	1.7043
VTH	735.5207m	755.2692m	528.1042m	-884.0359m
VDSAT	133.7757m	144.9151m	190.5888m	-240.9809m
BETA	9.5231m	7.5955m	3.6920m	2.5829m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	-1.0257m	922.3087u	-660.3693u	-562.1501u
GDS	-1.4882u	2.4455u	-2.6104u	-8.6584u
GMB	-241.5812u	211.8664u	-203.0503u	-88.8176u
GBD	3.6360f	2.9691f	2.9268f	1.8082f
GBS	3.6360f	2.9691f	2.9268f	1.8082f
CDTOT	93.6047f	47.6639f	122.8706f	88.3780f
CGTOT	92.0502f	74.4843f	145.4214f	73.6408f
CSTOT	49.6392f	82.4128f	45.0346f	49.4817f
CBTOT	105.1575f	98.7679f	125.1277f	102.3512f
CGS	10.8494f	60.9699f	8.7718f	9.4105f
CGD	74.8149f	8.6920f	125.3106f	60.9076f
CGB	6.3859f	4.8224f	11.3390f	3.3227f
CBD	45.7437f	38.9564f	42.2333f	51.5927f
CBS	38.7696f	43.6566f	36.2738f	40.0211f

	8	9	10	11
	M9	M10	M11	M12
MODEL	MODP	MODP	MODP	MODP
TYPE	PMOS	PMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	72.2288u	-74.5161u	74.5184u	-72.2289u
IBS	1.1421f	0.	1.9466f	0.
IBD	0.	1.9466f	0.	1.1415f
VGS	-455.4581m	-1.1021	0.	-1.1021
VDS	646.5975m	-1.1021	1.1021	-646.2704m
VBS	646.5975m	0.	1.1021	0.
VTH	-756.9193m	-756.8686m	-756.8686m	-756.9194m
VDSAT	-335.1792m	-335.2223m	-335.2273m	-335.1842m
BETA	1.2481m	1.2481m	1.2481m	1.2481m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	-372.5530u	384.9172u	-384.9227u	372.5456u
GDS	-6.2916u	4.2206u	-4.2207u	6.2949u
GMB	-80.2151u	82.9151u	-82.9163u	80.2135u
GBD	1.7663f	1.7663f	1.7663f	1.7663f
GBS	1.7663f	1.7663f	1.7663f	1.7663f
CDTOT	126.6186f	45.7984f	126.5529f	50.6581f
CGTOT	141.0053f	140.7716f	140.7716f	141.0058f
CSTOT	50.6536f	126.5529f	45.7984f	126.6187f
CBTOT	124.9793f	120.2358f	120.2357f	124.9834f
CGS	9.7219f	123.5067f	9.5320f	123.5934f
CGD	123.5933f	9.5320f	123.5068f	9.7224f
CGB	7.6901f	7.7328f	7.7328f	7.6900f
CBD	52.7129f	36.2697f	52.7129f	40.9918f
CBS	40.9877f	52.7129f	36.2696f	52.7129f

	12
	M13
MODEL	MODP
TYPE	PMOS
REGION	Saturation
ID	-72.2289u
IBS	1.1686f
IBD	3.0370f
VGS	-1.0967
VDS	-1.0333
VBS	646.2704m
VTH	-884.0454m
VDSAT	-241.2571m
BETA	2.5828m
RS	0.
RD	0.
GM	561.5324u
GDS	8.7723u
GMB	88.7251u
GBD	1.8082f
GBS	1.8082f
CDTOT	49.6701f
CGTOT	73.6428f
CSTOT	88.3846f
CBTOT	102.5454f
CGS	60.9091f
CGD	9.4110f
CGB	3.3228f
CBD	40.2090f
CBS	51.5980f

Figure 88: Small signal parameters of single stage mirrored cascode OTA.

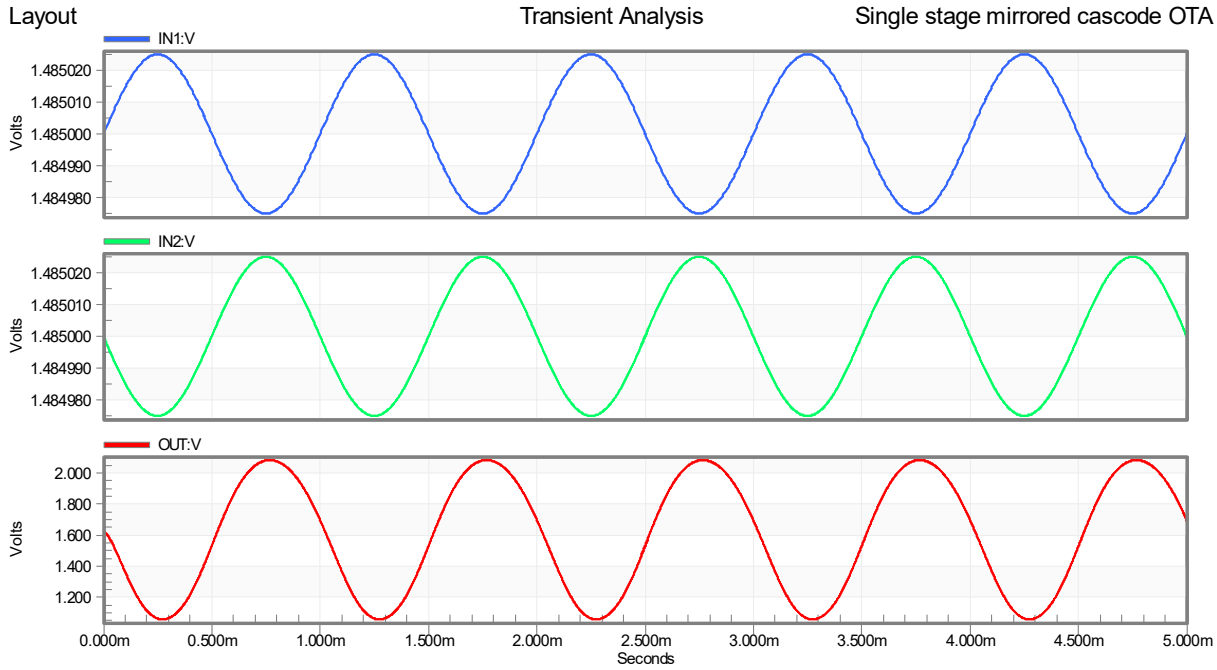
Figure 89 shows the AC analysis of single stage mirrored cascode. The circuit has a maximum gain around 80dB or Av=10000. The unity gain bandwidth bandwidth (ft) of the amplifier is around 63.9Mhz and this can be found when the characteristic of gain reaches 0dB. At 0dB the bandwidth frequency provides us information about the phase margin (PM). Because the phase margin is above 45° this means that the system is stable and in the output response we have no ringing. The bandwidth of the amplifier is determined by the -3dB which is the dominant pole at frequency of 6.3kHz as shown in (Fig. 89).




```
Measurement result summary
   Av_dB              =   80.7762
   PM                 =   51.6846
   ft                 =   63.9760MEG
   minus_threedb_pole =    6.3871k
```

Figure 89: AC analysis of single stage mirrored cascode OTA.

Figure 90 shows the transient analysis of single stage mirrored cascode OTA. By looking the peak to peak output trace voltage we see that the input signal is amplified as many times as the gain we extracted before. Figure 91 shows the power dissipation of the circuit at around 0.96mW. Table 9 shows the desired and the achieved performance characteristics of the amplifier.



Trace Name	Y1	Y2	Delta
IN1:V	1.49	1.49	-49.58u
IN2:V	1.49	1.49	49.58u
OUT:V	1.06	2.08	1.03

Figure 90: Transient analysis of single stage mirrored cascode OTA.

```
Average power consumed -> 9.684113e-04 watts
```

Figure 91: Power dissipation single stage mirrored cascode OTA.

Performance Specifications	Desired Values	Simulation Values
Overall Gain (A_V) (dB)	80	80
Unity Gain Bandwidth (GBW) (Mhz)	≥50	63.9
Phase Margin (PM) (°)	≥50	51
Power Dissipation (P_{diss}) (mW)	1	0.9

Table 9: Performance results of single stage mirrored cascode OTA.

4.2 Two Stage Operational Amplifier

Performance Specifications	Desired Values
VDD (V)	3.3
Overall Gain (A_V) (dB)	70
Unity Gain Bandwidth (GBW) (Mhz)	≥70
Phase Margin (PM) (°)	≥45
Power Dissipation (P_{diss}) (mW)	1
Output Voltage Swing (V)	0.3-1.5
Slew Rate (V/μs)	20
Compensation Capacitance (C_L) (pF)	2

Table 10: Two stage operational amplifier specifications.

The total bias current permitted: $I_{bias} = \frac{1mW}{3.3V} = 300\mu A$. Suppose that the current on the second stage must be twice the one in the input differential pair. With that M5 has $I_5 = 100\mu A$ current and M8 $I_8 = 200\mu A$. Using the equation that defines the proper transconductance by trying to achieve the proper bandwidth $g_{m4} = 2\pi f_T C_c = 2 \cdot \pi \cdot 70 \cdot 10^6 \cdot 2 \cdot 10^{-12} = 879.64\mu S$. For 0.35μm the minimum allowed gate length will be 0.7μm to ensure a proper function. Starting to increase the width of the transistor we derive the following results for the input transistor (Fig. 92).

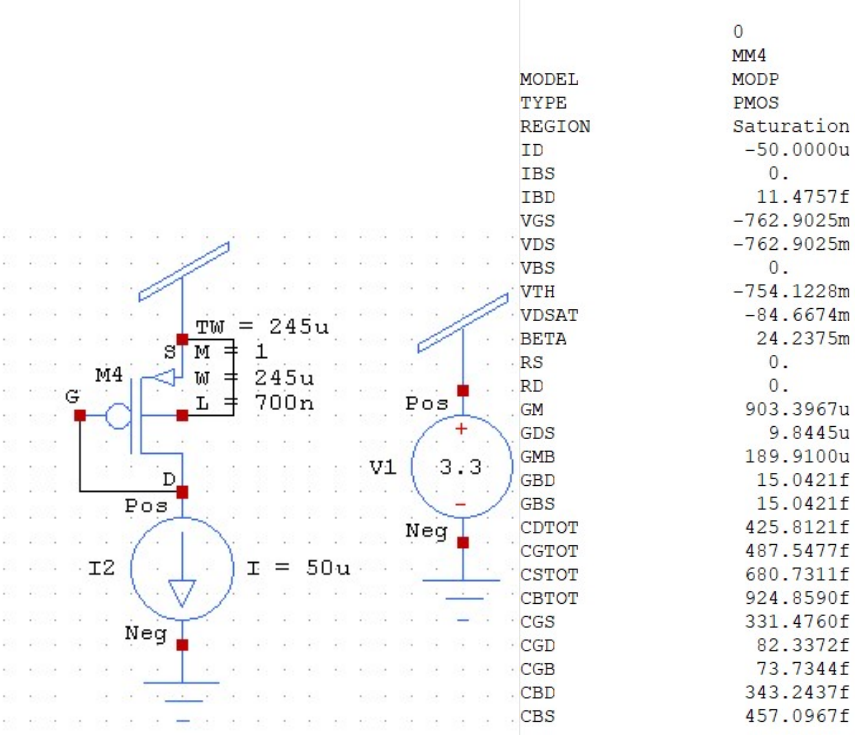
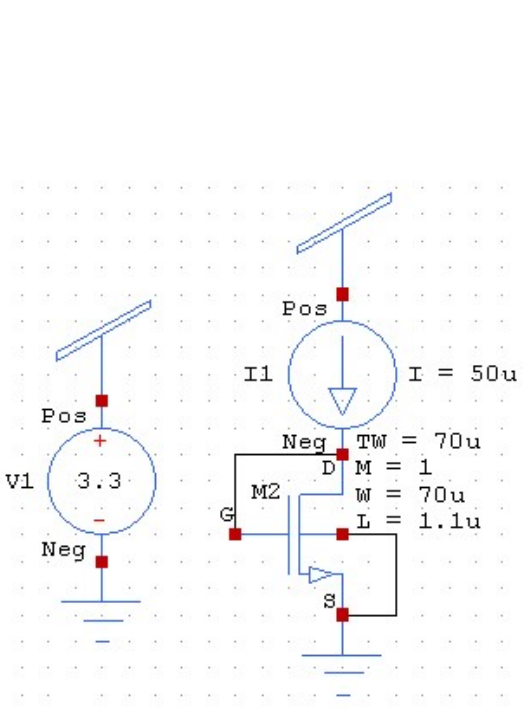


Figure 92: Transconductance calculation for the input transistor.

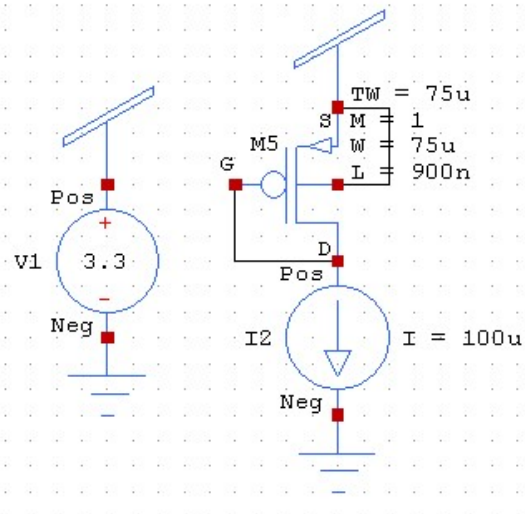
The lengths of active load M1 and M2 should be longer than the input pair so we choose $L_{n1} = L_{n2} = 1.1\mu m$. Increasing the width of M1 and M2 we accomplish the lower margin for the output swing close to 0.2V (Fig. 93).



	0
	MM2
MODEL	MODN
TYPE	NMOS
REGION	Saturation
ID	50.0000u
IBS	0.
IBD	-4.3334f
VGS	603.4442m
VDS	603.4442m
VBS	0.
VTH	533.1427m
VDSAT	102.8163m
BETA	11.9313m
RS	0.
RD	0.
GM	810.2466u
GDS	2.2611u
GMB	251.6480u
GBD	7.1811f
GBS	7.1811f
CDTOT	113.3911f
CGTOT	267.6568f
CSTOT	246.9922f
CBTOT	285.5834f
CGS	216.0369f
CGD	21.7862f
CGB	29.8338f
CBD	91.6144f
CBS	104.6868f

Figure 93: Calculation for the active load.

M3 must have the same length as M2 and M1. To ensure the lower output swing we match the overdrive voltages. For the differential sink transistor M5 we use a length 0.9μm. We increase the width of the transistor to achieve the minimum upper output swing close to 0.2V by considering a bias current 100μA (Fig. 94). Following the same process for M8 but now with a current of 200μA. Finally for our circuit bias transistor we match the overdrive voltage with M5 and M8 but we use a current of 300μA. The schematic design is shown in (Fig. 95) and its layout is shown in (Fig. 96). Figure 97 shows the small signal parameters of two stage operational amplifier. On APPENDIX B we can study the Netlist of the circuit (Netlist 15).



	0
	MM5
MODEL	MODP
TYPE	PMOS
REGION	Saturation
ID	-100.0000u
IBS	0.
IBD	4.3034f
VGS	-927.1098m
VDS	-927.1098m
VBS	0.
VTH	-756.5318m
VDSAT	-195.0273m
BETA	5.5355m
RS	0.
RD	0.
GM	941.4230u
GDS	10.3748u
GMB	201.1329u
GBD	4.6417f
GBS	4.6417f
CDTOT	126.1016f
CGTOT	247.4821f
CSTOT	268.3677f
CBTOT	292.7835f
CGS	207.4568f
CGD	25.2733f
CGB	14.7520f
CBD	100.7685f
CBS	140.2983f

Figure 94: Biasing transistor for the differential pair.

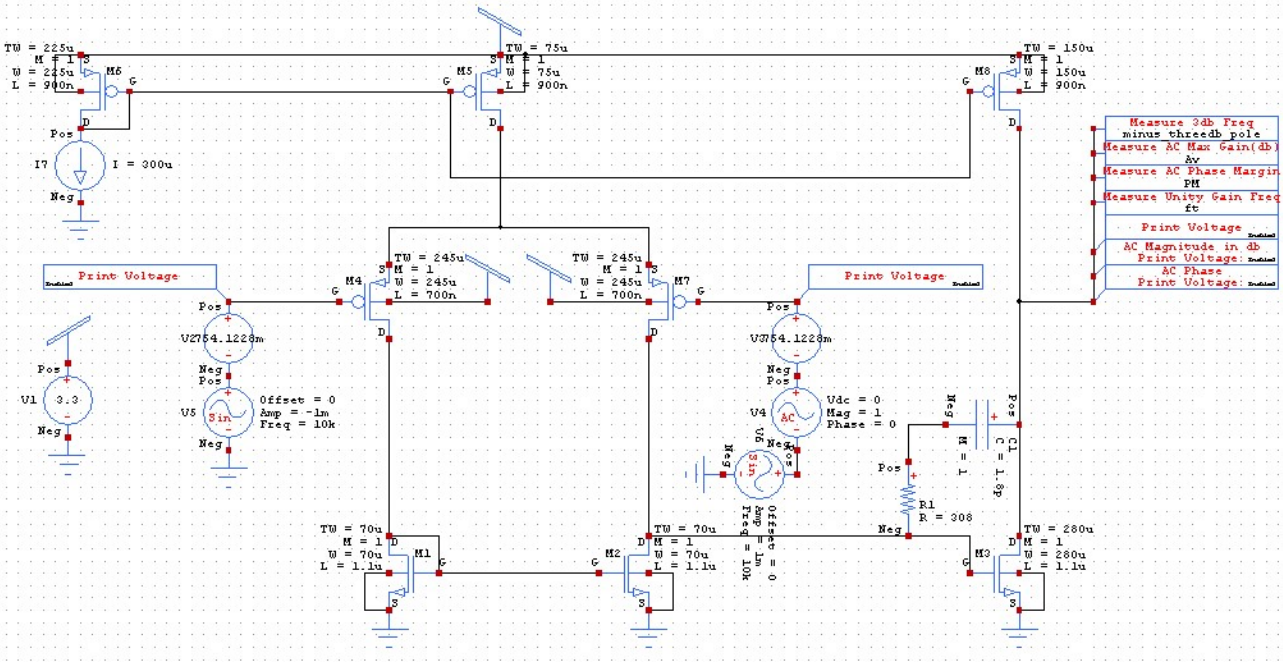


Figure 95: Schematic design of a two stage operational amplifier.

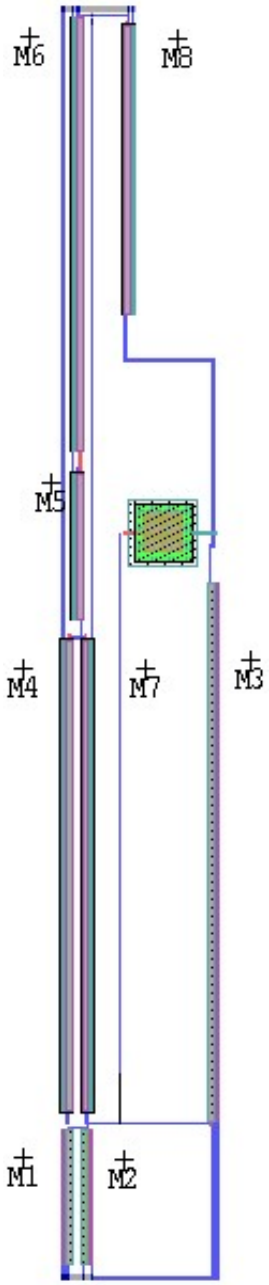


Figure 96: Layout design of a two stage operational amplifier.

AC SMALL-SIGNAL MODELS: temperature=25.0

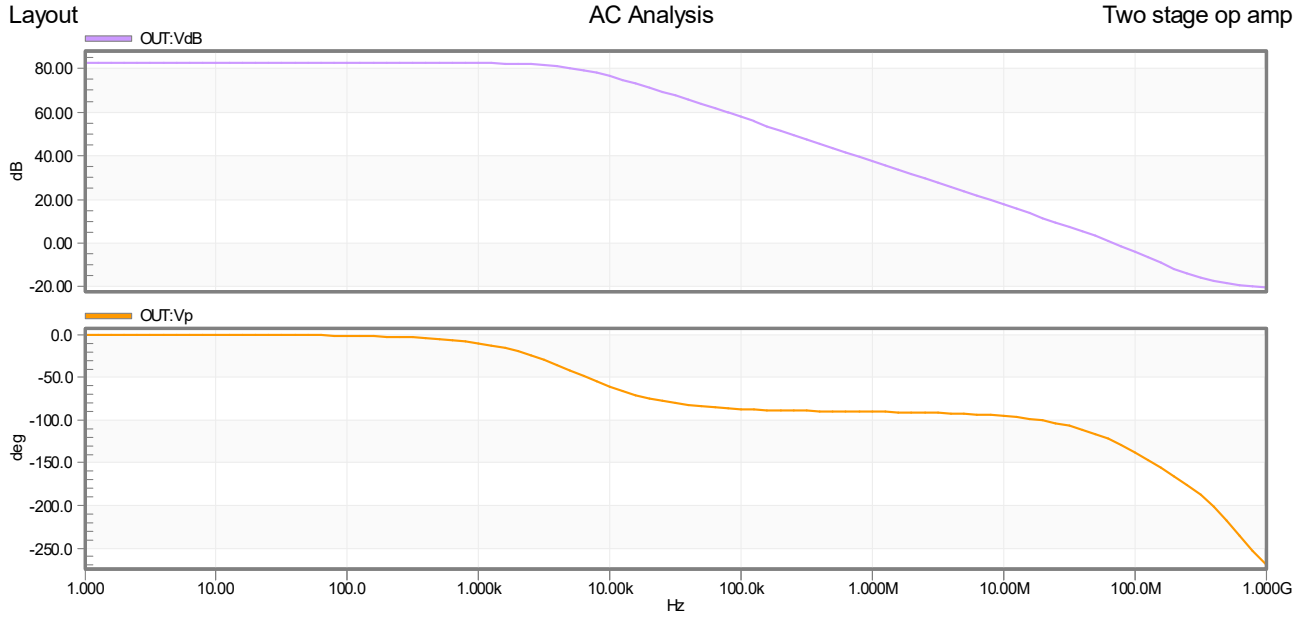
	0	1	2	3
	M1	M2	M3	M4
MODEL	MODN	MODN	MODN	MODP
TYPE	NMOS	NMOS	NMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	50.3303u	50.3303u	-219.9235u	50.3303u
IBS	0.	0.	-31.3414f	40.5558f
IBD	-4.3363f	-4.3363f	0.	23.2437f
VGS	603.8497m	603.8497m	-497.6718m	150.2731m
VDS	603.8497m	603.8497m	-1.1015	1.1509
VBS	0.	0.	-1.1015	2.6962
VTH	533.1427m	533.1427m	528.8746m	-993.5230m
VDSAT	103.0664m	103.0664m	105.9082m	-88.8642m
BETA	11.9312m	11.9312m	47.8000m	22.9469m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	814.2177u	814.2177u	-3.4857m	-927.3638u
GDS	2.2733u	2.2733u	-6.0024u	-8.4302u
GMB	252.8694u	252.8694u	-1.0808m	-114.5492u
GBD	7.1811f	7.1811f	28.4528f	15.0421f
GBS	7.1811f	7.1811f	28.4528f	15.0421f
CDTOT	113.3851f	113.3851f	992.2302f	496.7752f
CGTOT	267.8637f	267.8637f	1.0771p	459.5947f
CSTOT	247.1618f	247.1618f	426.7990f	319.8202f
CBTOT	285.5880f	285.5880f	1.1141p	597.4231f
CGS	216.3135f	216.3135f	86.8667f	82.3529f
CGD	21.7863f	21.7863f	873.5397f	330.8036f
CGB	29.7639f	29.7639f	116.7372f	46.4382f
CBD	91.6083f	91.6083f	416.9543f	285.5881f
CBS	104.6868f	104.6868f	339.9362f	237.2209f

	4	5	6	7
	M5	M6	M7	M8
MODEL	MODP	MODP	MODP	MODP
TYPE	PMOS	PMOS	PMOS	PMOS
REGION	Saturation	Saturation	Saturation	Saturation
ID	-100.6606u	-300.0000u	-50.3303u	219.9235u
IBS	0.	0.	23.2437f	20.2922f
IBD	7.1727f	12.7381f	40.5558f	0.
VGS	-921.8136m	-921.8136m	-1.0006	1.2767
VDS	-1.5452	-921.8136m	-1.1509	2.1985
VBS	0.	0.	1.5452	2.1985
VTH	-755.8943m	-752.3293m	-993.5230m	-752.1060m
VDSAT	-191.1750m	-194.9239m	-88.8642m	-194.9012m
BETA	5.5388m	16.7228m	22.9469m	11.1320m
RS	0.	0.	0.	0.
RD	0.	0.	0.	0.
GM	960.0921u	2.8382m	927.3638u	-2.0462m
GDS	8.4073u	31.2794u	8.4302u	-16.1593u
GMB	205.3208u	605.8764u	114.5492u	-437.6466u
GBD	4.6418f	13.8185f	15.0421f	9.2301f
GBS	4.6418f	13.8185f	15.0421f	9.2301f
CDTOT	113.0029f	377.7908f	319.8202f	535.8013f
CGTOT	247.2640f	740.6516f	459.5947f	493.9321f
CSTOT	268.2240f	803.3849f	496.7752f	206.7592f
CBTOT	279.7229f	876.9361f	597.4231f	539.6918f
CGS	207.1918f	620.3099f	330.8036f	50.4482f
CGD	25.2528f	75.7212f	82.3529f	413.8041f
CGB	14.8195f	44.6205f	46.4382f	29.6798f
CBD	87.6849f	301.8917f	237.2209f	280.0623f
CBS	140.3002f	419.8263f	285.5881f	156.1793f

Figure 97: Small signal parameters of two stage operational amplifier.

Figure 98 shows the AC analysis of two stage operational amplifier. The circuit has a maximum gain around 82dB or Av= 13500. The unity gain bandwidth (ft) of the amplifier is around 70Mhz and this can be found when the characteristic of gain reaches 0dB. At 0dB the unity gain bandwidth frequency provides us information about the phase margin (PM). Looking the compensation capacitor we see that is reduced at 1.8pF. This is because of the miller effect. Reducing the compensation capacitor between the first and the second stage maintains stability for the system. This means that increases above 45° the phase margin. In this configuration we

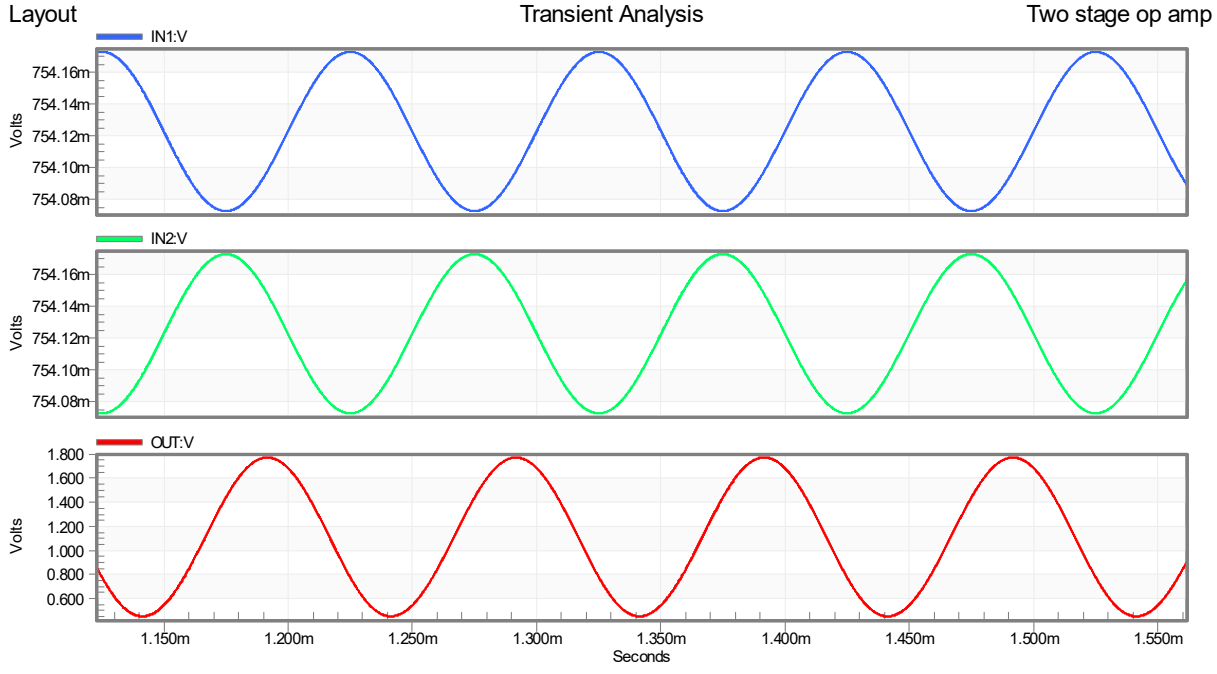
manage to achieve 55°. The bandwidth of the amplifier is determined by the -3dB which is the dominant pole at frequency of 5.6kHz as shown in (Fig. 98).




```
Measurement result summary
   Av_dB                =   82.6762
   PM                   = -125.1653
   ft                   =   69.8798MEG
   minus_threedb_pole   =    5.6002k
```

Figure 98: AC analysis of two stage operational amplifiers.

Figure 99 shows the transient analysis of two stage operational amplifier. By looking the peak to peak output trace voltage we see that the input signal is amplified as many times as the gain we extracted before. Figure 100 shows the power dissipation of the circuit around 1.8mW. Table 11 shows the desired and the simulated performance specifications of the amplifier.



Trace Name	Y1	Y2	Delta
IN1:V	754.15219m	754.102655m	-49.54u
IN2:V	754.09341m	754.142945m	49.54u
OUT:V	454.74198m	1.768880	1.31

Figure 99: Transient analysis of two stage operational amplifier.

```
Average power consumed -> 1.824469e-03 watts
```

Figure 100: Power dissipation of two stage operational amplifier.

Performance Specifications	Desired Values	Simulation Values
Overall Gain (A_V) (dB)	70	82
Unity Gain Bandwidth (GBW) (Mhz)	≥70	69.8
Phase Margin (PM) (°)	≥55	55
Power Dissipation (P_{diss}) (mW)	1	1.8

Table 11: Performance results of two stage operational amplifier.

CONCLUSIONS

The design choices for passive components, building blocks and operational amplifiers are based on careful consideration that a designer should be aware of. All design circuits should work for specific purpose based on designer choice and every circuit has its own advantages and disadvantages. The designer should be able to determine the most effective configuration for his application.

This thesis studied the essential components in integrated circuits, the single stage mirrored cascode OTA, and the two stage operational amplifier. The designing purpose of these circuits is similar with the references and bibliography. Some differences occur depending on SPICE models and the technology that has been chosen. Especially in passive components they can designed with different layer structures. But in general the designing point behind every component and circuit has the same role in final design.

The tools used in this thesis are valuable for design engineers in order to design, study and present the behaviour of circuit. For the schematic design the software tool is S-edit. For reading, writing netlists and extra commands in simulations the software tool is T-spice. For designing the layout the tool is L-edit. In schematic design the designer can make some simulations in order to understand the behaviour of the circuit. The technique for simulating and verify the behaviour of the circuit comes from the layout. First you design the layout with L-edit, extract the netlist and finally do the simulations on the layout design. If everything turn out as expected then the device is ready.

I take full responsibility for any errors and inaccuracies.

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APPENDIX A

Here you can find the SPICE files. They are suitable for simulations with the Tanner EDA software tools.

Level 1 model should be used in simple analysis and understanding.

For more accurate simulations it is better to use level 49 if the technology of 0.35μm is specifically used for the designs.

Spice simulation parameters for 0.5μm CMOS technology level 1

```
.MODEL MODN NMOS LEVEL=1
+ VTO=0.7e+00   GAMMA=0.45e+00   PHI=0.9e+00
+ NSUB=9.00e+14  LD=0.08e-06     UO=350e+00   LAMBDA=0.1
+ TOX=9.00e-09   PB=0.9e+00      CJ=0.56e-03  CJSW=0.35e-11
+ MJ=0.45e+00    MJSW=0.2e+00    CGDO=0.4e-09 JS=1.0e-08

.MODEL MODP PMOS LEVEL=1
+ VTO=-0.8e+00   GAMMA=0.4e+00    PHI=0.8e+00
+ NSUB=5.00e+14  LD=0.09e-06     UO=100e+00    LAMBDA=0.2
+ TOX=9.00e-09   PB=0.9e+00      CJ=0.94e-03   CJSW=0.32e-11
+ MJ=0.5e+00     MJSW=0.3e+00    CGDO=0.3e-09  JS = 0.5e-08
```

Spice simulation parameters for 0.35μm CMOS technology level 49

```
.MODEL MODN NMOS ( LEVEL = 49
+ version=3.1           binunit=1.0000e+00      mobmod=1
+ capmod=2              nqsmod=0.0000e+00
+ tox=7.7e-9            toxm=4.2000e-09
+ xj=1e-7                  nch=2.2e17           rsh=80
+ ngate=1.0000e+23       vth0=0.4739035
+ k1=0.5980711           k2=2.129508e-4        k3=89.1316051
+ k3b=-8.9451617         w0=3.267588e-5        nlx=2.389619e-7
+ dvt0=3.090362          dvt1=0.7427518        dvt2=-0.1500347
+ dvt0w=0                dvt1w=0               dvt2w=0
+ lint=0                 wint=1.45681e-7       dwg=-5.436366e-9
+ dwb=4.655955e-9        u0=385.646076
+ ua=-4.6434e-10         ub=2.099304e-18       uc=3.944494e-11
+ vsat=1.584114e5        a0=1.1776486          ags=0.1836559
+ b0=7.523723e-7         b1=5e-6               keta=2.991409e-3
+ a1=0                   a2=0.4259175          voff=-0.0938652
+ nfactor=1.3714105      cit=0                 cdsc=2.4e-4
+ cdscd=0                cdscb=0               eta0=0.9911705
+ etab=0.0151948         dsub=0.8661705        pclm=1.6432607
+ pdiblc1=1.509754e-3    pdiblc2=1.479156e-3   pdiblcb=0.1
+ drout=0                pscbe1=7.204688E8     pscbe2=6.67778e-4
+ pvag=0                 rdsw=1.060209e3       prwg=-0.0949099
```

```
+ prwb=-0.0949472        wr=1                    alpha0=0.0000e+00
+ alpha1=0.0000e+00      beta0=3.0000e+01        xpart=0.5
+ cgso=3.1e-10
+ cgdo=3.1e-10           cgbo=1e-12
+ cgsl=0.0000e+00        cgdl=0.0000e+00         ckappa=6.0000e-01
+ cf=0                   clc=1.0000e-07          cle=6.0000e-01
+ dlc=2.9000e-08         dwc=0.0000e+00          vfbcv=-1.0000e+00
+ noff=1.0000e+00        voffcv=0.0000e+00       acde=1.0000e+00
+ moin=1.5000e+01        lmin=1.8000e-07         lmax=5.0000e-05
+ wmin=2.4000e-07        wmax=1.0000e-04
+ xl=-5e-8
+ xw=1.5e-7              js=1.0000e-06
+ jsw=7.0000e-11         cj=9.161291e-4
+ mj=0.3472772           pb=0.8
+ cjsw=3.326018e-10                          mjsw=0.1126914
+ tnom=27                ute=-1.5                kt1=-0.11
+ kt1l=0                 kt2=0.022               ua1=4.31e-9
+ ub1=-7.61e-18          uc1=-5.6e-11            at=3.3e4
+ prt=0                  xti=3.0000e+00          wl=0
+ wln=1                  ww=0                    wwn=1
+ wwl=0                  ll=0                    lln=1
+ lw=0                   lwn=1                   lwl=0
+ llc=-2.1400e-15        lwc=0.0000e+00          lwlc=0.0000e+00
+ wlc=0.0000e+00         wwc=0.0000e+00          wwlc=0.0000e+00
+ lvth0=-1.0000e-03
+ wvth0=6.027e-02        pvth0=-0.0227383
+ lnlx=-2.8540e-08       wnlx=0.0000e+00         pnlx=0.0000e+00
+ wua=-1.8800e-11        wu0=5.4000e-01
+ pub=3.8000e-20         pw0=1.3000e-09          wrdsw=0.0000e+00
+ weta0=0.0000e+00       wetab=0.0000e+00        leta0=1.5740e-03
+ letab=0.0000e+00       peta0=0.0000e+00        petab=0.0000e+00
+ wpclm=0.0000e+00       wvoff=-4.0780e-04       lvoff=-4.2080e-03
+ pvoff=-3.7880e-04      wa0=-4.7310e-02         la0=-4.6670e-01
+ pa0=-2.6490e-02        wags=4.2420e-03         lags=3.0280e-01
+ pags=0.0000e+00        wketa=-1.530315e-3      lketa=-7.775726e-4
+ pketa=0.0000e+00       wute=6.3730e-02         lute=0.0000e+00
+ pute=0.0000e+00        wvsat=5.0660e+03        lvsat=0.0000e+00
+ pvsat=0.0000e+00       lpdiblc2=-4.7520e-03
+ wat=7.0670e+03         wprt=0.0000e+00         ldif=8.0000e-08
+ hdif=2.6000e-07        n=1.0000e+00            pbsw=0.8
+ cjswg=1.82e-10         ctp=9.1400e-04
+ ptp=9.2400e-04         cta=9.1900e-04          pta=1.5800e-03
+ elm=5.0000e+00         tlevc=1.0000e+00
+ noimod=2.0e+00         noia=1.3182567385564e+19        noib=144543.977074592
+ noic=-1.24515784572817e-12     ef=0.92                 em=41000000 )

.MODEL MODP PMOS ( LEVEL = 49
+ mobmod=1.0000e+00      version=3.1000e+00      capmod=2.0000e+00
+ binunit=1.0000e+00      nqsmod=0.0000e+00
+ tox=7.7e-9              toxm=4.2000e-09
+ xj=1e-7                 nch=8.52e+16            ngate=1.0000e+23
+ vth0= -0.7163484        k1=0.408893
+ k2=-4.658963e-3         k3=83.7384608           k3b=-5
+ w0=6.344557e-6          nlx=2.240363e-7         dvt0=1.6210073
+ dvt1=0.5540586          dvt2=4.208854e-4        dvt0w=0
```

```
+ dvt1w=0                dvt2w=0              lint=0
+ wint=1.472296E-7       dwg=-1.708734e-8     dwb=9.651369e-9
+ u0=152.1750181         ua=1.104005e-10
+ ub=1.869373e-18        uc=-1.72527e-11      vsat=1.303949e+5
+ a0=1.0511452           ags=0.3481503        b0=2.548932E-6
+ b1=5e-6                keta=-6.220316e-3    a1=1.304949e-4
+ a2=1.0000e+00          voff=-0.1353734      nfactor=1.8615508
+ cit=0                  cdsc=2.4e-4          cdscd=0
+ cdscb=0                eta0=0.0402356       etab=3.101076E-3
+ dsub=0.4414883         pclm=4.0879121       pdiblc1=1.7464E-4
+ pdiblc2=7.295654E-3    pdiblcb=0.049958     drout=9.989502e-4
+ pscbe1=7.963794e+10    pscbe2=5e-10         pvag=4.3044365
+ rdsw=4e+3              prwg=-0.1517701      prwb=0.0807754
+ alpha0=0.0000e+00      alpha1=0.0000e+00    beta0=3.0000e+01
+ cgdo=3.38e-10          cgbo=1e-12
+ cgso=3.38e-10          xpart=0.5
+ cf=0                   dlc=5.6000e-08       cgsl=0.0000e+00
+ cgdl=0.0000e+00        ckappa=6.0000e-01    clc=1.0000e-07
+ cle=6.0000e-01         dwc=0.0000e+00       vfbcv=-1.0000e+00
+ noff=1.0000e+00        voffcv=0.0000e+00    acde=1.0000e+00
+ moin=1.5000e+01        lmin=1.8000e-07      lmax=5.0000e-05
+ wmin=2.4000e-07        wmax=1.0000e-04
+ xl= -5e-8
+ xw=1.5E-7              js=3.0000e-06
+ jsw=4.1200e-11         cj=1.413045e-3
+ mj=0.5610227           pb=0.99
+ cjsw=2.971607e-10      mjsw=0.38282
+ tnom=2.7000e+01        ute=-1.5             kt1=-0.11
+ kt1l=0                 kt2=0.022            ua1=4.31e-9
+ ub1=-7.61e-18          uc1=-5.6e-11         at=3.3e+4
+ prt=0.0000e+00         xti=3.0000e+00       ww=0
+ lw=0                   ll=0                 wl=0.0000e+00
+ wln=1.0000e+00         wwn=1.0000e+00       wwl=0.0000e+00
+ lln=1.0000e+00         lwn=1.0000e+00       lwl=0.0000e+00
+ llc=-7.4500e-15        lwc=0.0000e+00       lwlc=0.0000e+00
+ wlc=0.0000e+00         wwc=0.0000e+00       wwlc=0.0000e+00
+ lvth0=4.4000e-03
+ wvth0=-1.4800e-02
+ pvth0=7.40325e-3       lnlx=-1.5840e-08
+ wrdsw=1.0070e+01       weta0=0.0000e+00     wetab=0.0000e+00
+ wpclm=0.0000e+00       wua=2.6300e-09       lua=-8.1530e-11
+ pua=5.8550e-11         wub=0.0000e+00       lub=0.0000e+00
+ pub=0.0000e+00         wuc=0.0000e+00       luc=0.0000e+00
+ puc=0.0000e+00         wvoff=-9.8160e-03    lvoff=-9.8710e-04
+ pvoff=-9.8330e-05      wa0=-4.8070e-02      la0=-2.8100e-01
+ pa0=8.6610e-02         wags=-4.1770e-02     lags=4.4540e-02
+ pags=-4.0760e-02       wketa=1.675253e-3    lketa=-3.463411e-3
+ pketa=0.0000e+00       wute=-2.6820e-01     lute=0.0000e+00
+ pute=0.0000e+00        wvsat=-1.4200e+04    lvsat=0.0000e+00
+ pvsat=-4.3400e+02      lpdiblc2=3.0120e-03
+ cjswg= 4.42E-11        wat=-6.4050e+03
+ wprt=2.1660e+02        n=1.0000e+00         pbsw=0.99
+ cta=1.0000e-03         ctp=7.5300e-04       pta=1.5500e-03
+ ptp=1.2400e-03         ldif=8.0000e-08      rsh=148.4
+ rd=0.0000e+00          rsc=0.0000e+00       rdc=0.0000e+00
```

```
+ hdif=2.6000e-07          rs=0.0000e+00
+ noimod=2.0e+00           noia=3.57456993317604e+18      noib=2500
+ noic=2.61260020285845e-11 ef=1.1388                     em=41000000 )
```

APPENDIX B

Code 1. Matlab calculation for M1 transistor process transconductance parameter

```
%process transconductance parameter for n-channel
tox=9*10^-9;                    %[m] spice referenced as TOX in [nm]
mn=350*10^-4;                   %[m^2/V-sec] spice referenced as UO in [cm^2/V-sec]
e0=8.858*10^-14*10^2;           %[F/m]
er_ox=3.9;                      %[]

Cox_result=Cox_function(e0,er_ox,tox);
kn_result=kn_function(mn,Cox_result);
fprintf('oxide capacitance: Cox=%d [F/m^2]\n',Cox_result);
fprintf('transconductance parameter for n-channel: kn=%d [A/V^2]\n',kn_result);

function kn_result=kn_function(mn,Cox)
kn_result=mn*Cox;
end

function Cox_result=Cox_function(e0,er_ox,tox)
Cox_result=(e0*er_ox)/tox;
end
```

Code 2. Matlab calculation for M1 transistor saturation current

```
%Calculation of ID n-channel in saturation region
Vth=700.0000*10^-3;     %[V]
Vgs=1.2;                %[V]
Vds=1.2;                %[V]
kn=1.343463*10^-4;      %[A/V^2]
L=2*10^-6;              %[m]
W=5*10^-6;              %[m]
lambda=0.1;             %[1/m]

Idnsaturation_result=Idnsaturation_function(kn,Vgs,Vth,W,L,lambda,Vds);
fprintf('ID n-channel in saturation region: Id=%d [A]\n',Idnsaturation_result);

function Idnsaturation_result=Idnsaturation_function(kn,Vgs,Vth,W,L,lambda,Vds)
Idnsaturation_result=(1/2)*kn*(W/L)*((Vgs-Vth)^2)*(1+lambda*Vds);
end
```

Code 3. Matlab calculation for M1 transistor transconductance parameter

```
%transconductance gm saturation region n-channel
Idsat=4.702120e-05;  %[A]
Vgs=1.2;                %[V]
Vth=700.0000*10^-3;     %[V]
gmsaturationn1_result=gmsaturationNtype1_function(Idsat,Vgs,Vth);
fprintf('transconductance saturation region n-channel: gm=%d
[A/V]\n',gmsaturationn1_result);

function gmsaturationn1_result=gmsaturationNtype1_function(Idsat,Vgs,Vth)
gmsaturationn1_result=(2*Idsat)/(Vgs-Vth);
end
```

Code 4. Matlab calculation for M1 transistor output conductance parameter

```
%calculation of output conductance gds n-channel saturation region
Idnsat=4.702120e-05;  %[A]
lambda=0.1;           %[1/m]
gdssaturationn_result=gdssaturationNtype_function(lambda,Idnsat);
```

```
fprintf('output conductance n-channel saturation region: gds=%d
[A/V]\n',gdssaturationn_result);

function gdssaturationn_result=gdssaturationNtype_function(lambda,Idnsat)
gdssaturationn_result=lambda*Idnsat;
end
```

Code 5. Matlab calculation for M4 process transconductance parameter

```
%process transconductance parameter for p-channel
tox=9*10^-9;                  %[m] spice referenced as TOX in [nm]
mp=100*10^-4;                 %[m^2/V-sec] spice referenced as UO in [cm^2/V-sec]
e0=8.858*10^-14*10^2;         %[F/m]
er_ox=3.9;                    %[]
Cox_result=Cox_function(e0,er_ox,tox);
kp_result=kp_function(mp,Cox_result);
fprintf('oxide capacitance: Cox=%d [F/m^2]\n',Cox_result);
fprintf('transconductance parameter for p-channel: kp=%d [A/V^2]\n',kp_result);

function kp_result=kp_function(mp,Cox)
kp_result=mp*Cox;
end

function Cox_result=Cox_function(e0,er_ox,tox)
Cox_result=(e0*er_ox)/tox;
end
```

Code 6. Matlab calculation for M4 transistor saturation current

```
%Calculation of ID p-channel in saturation region
Vth=-800.0000*10^-3;      %[V]
Vgs=-1.2;                 %[V]
Vds=-1.2;                 %[V]
L=2*10^-6;                %[m]
W=5*10^-6;                %[m]
kp=3.838467e-05;          %[A/V^2]
lambda=0.2;               %[1/m]

Idpsaturation_result=Idpsaturation_function(kp,W,L,Vgs,Vth,lambda,Vds);
fprintf('ID p-channel saturation region: Id=%d [A]\n',Idpsaturation_result);

function Idpsaturation_result=Idpsaturation_function(kp,W,L,Vgs,Vth,lambda,Vds)
Idpsaturation_result=(1/2)*kp*(W/L)*abs((Vgs-Vth)^2)*(1+lambda*abs(Vds));
end
```

Code 7. Matlab calculation for M4 transistor transconductance parameter

```
%transconductance gm saturation region p-channel
Idsat=9.519398e-06;  %[A]
Vgs=-1.2;              %[V]
Vth=-800.0000*10^-3; %[V]
gmsaturationp1_result=gmsaturationPtype1_function(Idsat,Vgs,Vth);
fprintf('transconductance saturation region p-channel: gm=%d
[A/V]\n',gmsaturationp1_result);

function gmsaturationp1_result=gmsaturationPtype1_function(Idsat,Vgs,Vth)
gmsaturationp1_result=(2*Idsat)/(abs(Vgs-Vth));
end
```

Code 8. Matlab calculation for M4 transistor output conductance parameter

```
%calculation of output conductance gds p-channel saturation region
Idpsat=9.519398e-06;  %[A]
lambda=0.2;           %[1/m]
gdssaturationp_result=gdssaturationPtype_function(lambda,Idpsat);
fprintf('output conductance p-channel saturation region gds=%d
[A/V]\n',gdssaturationp_result);
```

```
function gdssaturationp_result=gdssaturationPtype_function(lambda,Idpsat)
gdssaturationp_result=lambda*Idpsat;
end
```

Code 9. Error calculation Spice vs Matlab results

```
id1_calc=4.702120*10^-5;   %[A]
id1_spice=51.0880*10^-6;   %[A]
gm1_calc=1.880848*10^-4;   %[A/V]
gm1_spice=204.6989*10^-6;  %[A/V]
gds1_calc=4.702120*10^-6;  %[A/V]
gds1_spice=4.5614*10^-6;   %[A/V]
id4_calc=9.519398*10^-6;   %[A]
id4_spice=10.4564*10^-6;   %[A]
gm4_calc=4.759699*10^-5;   %[A/V]
gm4_spice=52.3828*10^-6;   %[A/V]
gds4_calc=1.903880*10^-6;  %[A/V]
gds4_spice=1.6865*10^-6;   %[A/V]

id1_percentage_error_result=id1_percentage_error_function(id1_calc,id1_spice);
fprintf('M1 current percentage error id1_error=%d%% \n',id1_percentage_error_result);
gm1_percentage_error_result=gm1_percentage_error_function(gm1_calc,gm1_spice);
fprintf('M1 transconductance percentage error gm1_error=%d%%
\n',gm1_percentage_error_result);
gds1_percentage_error_result=gds1_percentage_error_function(gds1_calc,gds1_spice);
fprintf('M1 output conductance percentage error
gds1_error=%d%%\n',gds1_percentage_error_result);
id4_percentage_error_result=id4_percentage_error_function(id4_calc,id4_spice);
fprintf('M4 current percentage error id4_error=%d%% \n',id4_percentage_error_result);
gm4_percentage_error_result=gm4_percentage_error_function(gm4_calc,gm4_spice);
fprintf('M4 transconductance percentage error gm4_error=%d%%
\n',gm4_percentage_error_result);
gds4_percentage_error_result=gds4_percentage_error_function(gds4_calc,gds4_spice);
fprintf('M4 output conductance percentage error gds4_error=%d%%
\n',gds4_percentage_error_result);

function id1_percentage_error_result=id1_percentage_error_function(id1_calc,id1_spice)
id1_percentage_error_result=abs((id1_calc-id1_spice)/id1_spice)*100;
end
function gm1_percentage_error_result=gm1_percentage_error_function(gm1_calc,gm1_spice)
gm1_percentage_error_result=abs((gm1_calc-gm1_spice)/gm1_spice)*100;
end
function
gds1_percentage_error_result=gds1_percentage_error_function(gds1_calc,gds1_spice)
gds1_percentage_error_result=abs((gds1_calc-gds1_spice)/gds1_spice)*100;
end
function id4_percentage_error_result=id4_percentage_error_function(id4_calc,id4_spice)
id4_percentage_error_result=abs((id4_calc-id4_spice)/id4_spice)*100;
end
function gm4_percentage_error_result=gm4_percentage_error_function(gm4_calc,gm4_spice)
gm4_percentage_error_result=abs((gm4_calc-gm4_spice)/gm4_spice)*100;
end
function
gds4_percentage_error_result=gds4_percentage_error_function(gds4_calc,gds4_spice)
gds4_percentage_error_result=abs((gds4_calc-gds4_spice)/gds4_spice)*100;
end
```

Code 10. Resistor calculation 308 ohm

```
W=0.34;          %[um]
L=25;            %[um]
rsquare=4.2;     %[ohms/square]

resistor_result=resistor_function(W,L,rsquare);
fprintf('Resistor=%d [Ohms]\n',resistor_result);
```

```
function resistor_result=resistor_function(W,L,rsquare)
resistor_result=(L/W)*rsquare;
end
Result: Resistor=3.088235e+02 [Ohms]
```

Code 11. Calculation of vertical squares

```
%calculating the number of squares needed vertically for the resistance
L_W_squares=238;                        %total squares needed
vertical_parts=8;                       %vertical squares based on serpentine structure
horizontal_parts=vertical_parts-1;      %horizontal squares calculation based on sepentine
structure
corners=horizontal_parts*2; %corner squares calculation based on
serpentine structure
vertical_squares_result=vertical_squares_function(L_W_squares,vertical_parts,horizontal_p
arts,corners);
fprintf('\nnumber of squares needed vertically for the resistance: vertical_squares=%d
[squares]\n',vertical_squares_result);

function
vertical_squares_result=vertical_squares_function(L_W_squares,vertical_parts,horizontal_p
arts,corners)
vertical_squares_result=(L_W_squares-horizontal_parts-corners/2)/vertical_parts;
end
Result: number of squares needed vertically for the resistance: vertical_squares=28
[squares]
```

Code 12. Calculation of 2pF capacitor using Matlab

```
%calculation of capacitor
e0=8.858*10^-14;        %[F/cm]
er_ox=3.9;
tox=7.7e-09*(10^2);     %[cm]
W=21;                   %[um]
L=21;                   %[um]
Cap_value=2*10^-12;   %[F]

Cox_result=Cox_function(e0,er_ox,tox);
fprintf('Oxide capacitance Cox=%d [F/um^2]\n',Cox_result)
Capacitor_result=Capacitor_function(Cox_result,W,L);
fprintf('capacitance C=%d [F]\n',Capacitor_result)
area_ratio_result=area_ratio_function(Cap_value,Cox_result);
fprintf('capacitor area=%d []\n',area_ratio_result)
fprintf('capacitor Width and length should be: %d each [um]\n',sqrt(area_ratio_result));

function Cox_result=Cox_function(e0,er_ox,tox)
Cox_result=((e0*er_ox)/tox)*(1/10^4)^2;
end

function Capacitor_result=Capacitor_function(Cox_result,W,L)
Capacitor_result=Cox_result*(W*L);
end

%calculating area of capacitor to extract the W and L
function area_ratio_result=area_ratio_function(Cap_value,Cox_result)
area_ratio_result=Cap_value/Cox_result;
end
Result: Oxide capacitance Cox=4.486519e-15 [F/um^2]
capacitance C=1.978555e-12 [F]
capacitor area=4.457799e+02 []
capacitor Width and length should be: 2.111350e+01 each [um]
```

Code 13. Cox capacitance for 0.35um

```
%calculation for Cox
```

```
e0=8.858*10^-14;     %[F/cm]
er_ox=3.9;           %[]
tox=9.00e-09*(10^2); %[cm]
Cox_result=Cox_function(e0,er_ox,tox);
fprintf('Oxide capacitance Cox=%d [F/cm^2]\n',Cox_result)


function Cox_result=Cox_function(e0,er_ox,tox)
Cox_result=(e0*er_ox)/tox;
end
Result: Oxide capacitance Cox=3.838467e-07 [F/cm^2]
```

Code 14. Ron_max resistance calculation

```
%calculating Ron resistance
W_L=2.5;             %aspect ratio
mn=350e+00;          %[cm^2/Vsec]
Cox=3.838467e-07;    %[F/cm^2]
kn=mn*Cox;           %[A/V^2]
Vg=3.3;              %[V]
Vs=1.3;                %[V]
Vth=700*10^-3;       %[V]
Vov=(Vg-Vs)-Vth;     %[V]

Ron_result=Ron_function(W_L,kn,Vov);
fprintf('\nMOS on-resistance Ron=%d[Ohm]\n',Ron_result);

function Ron_result=Ron_function(W_L,kn,Vov)
    Ron_result=1/(kn*W_L*abs(Vov));
end
Result: MOS on-resistance Ron=2.290292e+03[Ohm]
```

Code 15. Ron_min resistance calculation

```
%calculating Ron resistance
W_L=2.5;             %aspect ratio
mn=350e+00;          %[cm^2/Vsec]
Cox=3.838467e-07;    %[F/cm^2]
kn=mn*Cox;           %[A/V^2]
Vg=3.3;              %[V]
Vs=0;                %[V]
Vth=700*10^-3;       %[V]
Vov=(Vg-Vs)-Vth;     %[V]

Ron_result=Ron_function(W_L,kn,Vov);
fprintf('\nMOS on-resistance Ron=%d[Ohm]\n',Ron_result);

function Ron_result=Ron_function(W_L,kn,Vov)
    Ron_result=1/(kn*W_L*abs(Vov));
end

Result: MOS on-resistance Ron=1.145146e+03[Ohm]
```

Code 16. Time constant calculation

```
%calculating RC time constant
C=2*10^-12;                %[F]
R=1.860862e+03;            %[Ohm]


TC_result=TC_function(R,C);
fprintf('\ntime constant: TC=%d [sec]\n',TC_result);

function TC_result=TC_function(R,C)
TC_result=R*C;
end
```

```
Result: time constant: TC=4.580584e-09 [sec]
```

Code 17. Charge stored in channel of NMOS

```
%charge stored in channel of an n-channel transistor in on state
W=2.5;                        %[um]
L=1;                          %[um]
Cox=3.838467e-07*(1/10^4)^2; %[F/um^2]
Vg=3.3;                       %[V]
Vth=0.7;                      %[V]
Vs=1.3;                       %[V]
Qch_Ntype_result=Qch_Ntype_function(W,L,Cox,Vg,Vs,Vth);
fprintf('\nThe charge stored in channel of NMOS transistor in on state: Qch_Ntype=%d
[Coulomb]\n',Qch_Ntype_result);

function Qch_Ntype_result=Qch_Ntype_function(W,L,Cox,Vg,Vs,Vth)
     Qch_Ntype_result=W*L*Cox*abs((Vg-Vs)-Vth);
end
Result: The charge stored in channel of NMOS transistor in on state: Qch_Ntype=1.247502e-
14 [Coulomb]
```

Code 18. Charge stored in channel of complementary transistor

```
%charge for complementary transistors
W1=5;                             %[um]
L1=1;                             %[um]
W2=2.5;                           %[um]
L2=1;                             %[um]
Cox=3.838467e-07*(1/10^4)^2;      %[F/um^2]
Vg=3.3;                           %[V]
Vth=0.7;                          %[V]
Vs=1.3;                           %[V]
Qch_Ntype_result=Qch_Ntype_function(W1,L1,Cox,Vg,Vs,Vth);
fprintf('\nThe charge stored in channel of NMOS transistor in on state: Qch_Ntype=%d
[Coulomb]\n',Qch_Ntype_result);

Qch_Ptype_result=Qch_Ptype_function(W2,L2,Cox,Vg,Vth);
fprintf('\nThe charge stored in channel of PMOS transistor in on state: Qch_Ptype=%d
[Coulomb]\n',Qch_Ptype_result);

function Qch_Ntype_result=Qch_Ntype_function(W1,L1,Cox,Vg,Vs,Vth)
     Qch_Ntype_result=W1*L1*Cox*abs((Vg-Vs)-Vth);
end

function Qch_Ptype_result=Qch_Ptype_function(W2,L2,Cox,Vg,Vth)
     Qch_Ptype_result=W2*L2*Cox*abs(Vg-Vth);
end
Result: The charge stored in channel of NMOS transistor in on state: Qch_Ntype=2.495004e-
14 [Coulomb]

The charge stored in channel of PMOS transistor in on state: Qch_Ptype=2.495004e-14
[Coulomb]
```

Code 19. AC analysis calculation using Matlab for push-pull inverter

```
%Small Signal Analysis
Cgs1=16.0591*10^-15;        %[F]
Cgd1=2.2143*10^-15;         %[F]
Cdb1=8.8894*10^-15;         %[F]
Cdb2=7.7782*10^-15;         %[F]
Cgd2=2.3918*10^-15;         %[F]
CL=0.5*10^-12;              %[F]
gm1=859.3620*10^-6;         %[A/V]
gm2=423.2316*10^-6;         %[A/V]
gds1=9.7816*10^-6;          %[A/V]
gds2=20.0300*10^-6;         %[A/V]
```

```
C1_result=C1_function(Cgs1);
fprintf('C1=%d [F]\n',C1_result);
C2_result=C2_function(Cgd1);
fprintf('C2=%d [F]\n',C2_result);
C3_result=C3_function(Cdb1,Cdb2,Cgd2,CL);
fprintf('C3=%d [F]\n',C3_result);
R1_result=R1_function(gds1);
fprintf('R1=%d [Ohms]\n',R1_result);
R2_result=R2_function(gds2);
fprintf('R2=%d [Ohms]\n',R2_result);
Av1_result=Av1_function(gm1,gds1,gds2);
fprintf('Av1=%d [V/V]\n',Av1_result);
fp_out_result=fp_out_function(gds1,gds2,C2_result,C3_result);
fprintf('pole1 fp_out=%d [Hz]\n',fp_out_result);
fT_result=fT_function(gm1,C2_result,C3_result);
fprintf('unity gain frequency fT=%d [Hz]\n',fT_result);
db_result=db_function(Av1_result);
fprintf('dB=%d [dB]\n',db_result);


function C1_result=C1_function(Cgs1)
C1_result=Cgs1;
end
function C2_result=C2_function(Cgd1)
C2_result=Cgd1;
end
function C3_result=C3_function(Cdb1,Cdb2,Cgd2,CL)
C3_result=Cdb1+Cdb2+Cgd2+CL;
end
function Av1_result=Av1_function(gm1,gds1,gds2)
Av1_result=-gm1/(gds1+gds2);
end
function R1_result=R1_function(gds1)
R1_result=1/gds1;
end
function R2_result=R2_function(gds2)
R2_result=1/gds2;
end
function fp_out_result=fp_out_function(gds1,gds2,C2_result,C3_result)
fp_out_result=(gds1+gds2)/((2*pi)*(C2_result+C3_result));
end
function fT_result=fT_function(gm1,C2_result,C3_result)
fT_result=(1/(2*pi))*(gm1/(C2_result+C3_result));
end
function db_result=db_function(Av1_result)
db_result=20*log10(-Av1_result);
end
Result:
C1=1.605910e-14 [F]
C2=2.214300e-15 [F]
C3=5.190594e-13 [F]
R1=1.022328e+05 [Ohms]
R2=4.992511e+04 [Ohms]
Av1=-2.882643e+01 [V/V]
pole1 fp_out=9.102058e+06 [Hz]
unity gain frequency fT=2.623798e+08 [Hz]
dB=2.919582e+01 [dB]
```

Code 20. AC analysis calculation using Matlab for inverter with active load

```
%Small Signal Analysis
Cgs1=63.3038*10^-15;          %[F]
Cgd1=10.8594*10^-15;          %[F]
Cdb1=58.9654*10^-15;          %[F]
Cdb2=61.2600*10^-15;          %[F]
Cgd2=9.5084*10^-15;           %[F]
CL=0.5*10^-12;                %[F]
gm1=542.4882*10^-6;           %[A/V]
gm2=254.6113*10^-6;           %[A/V]
```

```
gds1=674.5822*10^-9;          %[A/V]
gds2=1.6723*10^-6;            %[A/V]

C1_result=C1_function(Cgs1);
fprintf('C1=%d [F]\n',C1_result);
C2_result=C2_function(Cgd1);
fprintf('C2=%d [F]\n',C2_result);
C3_result=C3_function(Cdb1,Cdb2,Cgd2,CL);
fprintf('C3=%d [F]\n',C3_result);
R1_result=R1_function(gds1);
fprintf('R1=%d [Ohms]\n',R1_result);
R2_result=R2_function(gds2);
fprintf('R2=%d [Ohms]\n',R2_result);
Av1_result=Av1_function(gm1,gds1,gds2);
fprintf('Av1=%d [V/V]\n',Av1_result);
fp_out_result=fp_out_function(gds1,gds2,C2_result,C3_result);
fprintf('pole1 fp_out=%d [Hz]\n',fp_out_result);
fT_result=fT_function(gm1,C2_result,C3_result);
fprintf('unity gain frequency fT=%d [Hz]\n',fT_result);
db_result=db_function(Av1_result);
fprintf('dB=%d [dB]\n',db_result);


function C1_result=C1_function(Cgs1)
C1_result=Cgs1;
end
function C2_result=C2_function(Cgd1)
C2_result=Cgd1;
end
function C3_result=C3_function(Cdb1,Cdb2,Cgd2,CL)
C3_result=Cdb1+Cdb2+Cgd2+CL;
end
function Av1_result=Av1_function(gm1,gds1,gds2)
Av1_result=-gm1/(gds1+gds2);
end
function R1_result=R1_function(gds1)
R1_result=1/gds1;
end
function R2_result=R2_function(gds2)
R2_result=1/gds2;
end
function fp_out_result=fp_out_function(gds1,gds2,C2_result,C3_result)
fp_out_result=(gds1+gds2)/((2*pi)*(C2_result+C3_result));
end
function fT_result=fT_function(gm1,C2_result,C3_result)
fT_result=(1/(2*pi))*(gm1/(C2_result+C3_result));
end
function db_result=db_function(Av1_result)
db_result=20*log10(-Av1_result);
end
Result:
C1=6.330380e-14 [F]
C2=1.085940e-14 [F]
C3=6.297338e-13 [F]
R1=1.482399e+06 [Ohms]
R2=5.979788e+05 [Ohms]
Av1=-2.311527e+02 [V/V]
pole1 fp_out=5.830813e+05 [Hz]
unity gain frequency fT=1.347808e+08 [Hz]
dB=4.727798e+01 [dB]
```

Code 21. AC analysis calculation using Matlab for cascode with active load

```
%Small Signal Analysis
Cgs1=63.0104*10^-15;        %[F]
Cgd1=10.8679*10^-15;        %[F]
Cdb1=46.0677*10^-15;        %[F]
Cdb2=38.3832*10^-15;        %[F]
Cdb3=37.5191*10^-15;        %[F]
```

```
Cgd2=10.8575*10^-15;        %[F]
Cgd3=9.5237*10^-15;         %[F]
Cgs2=63.0030*10^-15;        %[F]
Csb2=46.0677*10^-15;        %[F]
CL=0.5*10^-12;              %[F]
gm1=525.2004*10^-6;         %[A/V]
gm2=535.1937*10^-6;         %[A/V]
gds1=1.6991*10^-6;          %[A/V]
gds2=662.3123*10^-9;        %[A/V]
gds3=1.9641*10^-6;          %[A/V]

C1_result=C1_function(Cgs1);
fprintf('C1=%d [F]\n',C1_result);
C2_result=C2_function(Cgd1);
fprintf('C2=%d [F]\n',C2_result);
C3_result=C3_function(Cgd2,Cgd3,Cdb2,Cdb3,CL);
fprintf('C3=%d [F]\n',C3_result);
C4_result=C4_function(Cgs2,Cdb1,Csb2);
fprintf('C4=%d [F]\n',C4_result);
R1_result=R1_function(gds1);
fprintf('R1=%d [Ohms]\n',R1_result);
R2_result=R2_function(gds2);
fprintf('R2=%d [Ohms]\n',R2_result);
Av1_result=Av1_function(gm1,gds3);
fprintf('Av1=%d [V/V]\n',Av1_result);
Av2_result=Av2_function(gm1,gm2);
fprintf('node 1 Av2=%d [V/V]\n',Av2_result);
fp_out_result=fp_out_function(gds3,C3_result);
fprintf('pole fp_out=%d [Hz]\n',fp_out_result);
fT_result=fT_function(gm1,C3_result);
fprintf('unity gain frequency fT=%d [Hz]\n',fT_result);
db_result=db_function(Av1_result);
fprintf('dB=%d [dB]\n',db_result);

function C1_result=C1_function(Cgs1)
C1_result=Cgs1;
end
function C2_result=C2_function(Cgd1)
C2_result=Cgd1;
end
function C3_result=C3_function(Cgd2,Cgd3,Cdb2,Cdb3,CL)
C3_result=Cgd2+Cgd3+Cdb2+Cdb3+CL;
end
function C4_result=C4_function(Cgs2,Cdb1,Csb2)
C4_result=Cgs2+Cdb1+Csb2;
end
function Av1_result=Av1_function(gm1,gds3)
Av1_result=-gm1/gds3;
end
function Av2_result=Av2_function(gm1,gm2)
Av2_result=-gm1/gm2;
end
function R1_result=R1_function(gds1)
R1_result=1/gds1;
end
function R2_result=R2_function(gds2)
R2_result=1/gds2;
end
function fp_out_result=fp_out_function(gds3,C3_result)
fp_out_result=(1/(2*pi))*(gds3/C3_result);
end
function fT_result=fT_function(gm1,C3_result)
fT_result=(1/(2*pi))*(gm1/C3_result);
end
function db_result=db_function(Av1_result)
db_result=20*log10(-Av1_result);
end
Result:
```

```
C1=6.301040e-14 [F]
C2=1.086790e-14 [F]
C3=5.962835e-13 [F]
C4=1.551384e-13 [F]
R1=5.885469e+05 [Ohms]
R2=1.509862e+06 [Ohms]
Av1=-2.674000e+02 [V/V]
node 1 Av2=-9.813277e-01 [V/V]
pole fp_out=5.242409e+05 [Hz]
unity gain frequency fT=1.401820e+08 [Hz]
dB=4.854323e+01 [dB]
```

Code 22. AC analysis calculation using Matlab for cascode with cascode load

```
%Small Signal Analysis
Cgs1=63.0101*10^-15;        %[F]
Cgd1=10.8679*10^-15;        %[F]
Cdb1=46.0791*10^-15;        %[F]
Cdb2=42.2471*10^-15;        %[F]
Cdb3=37.5316*10^-15;        %[F]
Cgd2=10.8637*10^-15;        %[F]
Cgd3=9.5237*10^-15;         %[F]
Cgs2=63.3188*10^-15;        %[F]
Csb2=46.0791*10^-15;        %[F]
Cgs3=122.6342*10^-15;       %[F]
Cgd4=122.6342*10^-15;       %[F]
Csb3=52.7129*10^-15;        %[F]
Cdb4=52.7129*10^-15;        %[F]
CL=0.5*10^-12;              %[F]
gm1=525.1546*10^-6;         %[A/V]
gm2=532.6640*10^-6;         %[A/V]
gm3=247.0962*10^-6;         %[A/V]
gm4=247.0998*10^-6;         %[A/V]
gds1=1.7047*10^-6;          %[A/V]
gds2=1.5884*10^-6;          %[A/V]
gds3=1.96528*10^-6;         %[A/V]
gds4=1.9650*10^-6;          %[A/V]

C1_result=C1_function(Cgs1);
fprintf('C1=%d [F]\n',C1_result);
C2_result=C2_function(Cgd1,Cdb1,Cgs2,Csb2);
fprintf('C2=%d [F]\n',C2_result);
C3_result=C3_function(Cgs3,Cgd4,Csb3,Cdb4);
fprintf('C3=%d [F]\n',C3_result);
Cout_result=Cout_function(Cgd2,Cgd3,Cdb2,Cdb3,CL);
fprintf('Cout=%d [F]\n',Cout_result);
Rpcascode_result=Rpcascode_function(gm3,gds3,gds4);
fprintf('Rpcascode=%d [Ohms]\n',Rpcascode_result);
Rncascode_result=Rncascode_function(gm2,gds2,gds1);
fprintf('Rncascode=%d [Ohms]\n',Rncascode_result);
Rout_result=Rout_function(Rpcascode_result,Rncascode_result);
fprintf('Rout=%d [Ohms]\n',Rout_result);
Av1_result=Av1_function(gm1,Rout_result);
fprintf('Av1=%d [V/V]\n',Av1_result);
Av2_result=Av2_function(gm1,gm2);
fprintf('node 1 Av2=%d [V/V]\n',Av2_result);
Av3_result=Av3_function(gm4,gm3);
fprintf('node 3 Av3=%d [V/V]\n',Av3_result);
fp_out_result=fp_out_function(Rout_result,Cout_result);
fprintf('pole fp_out=%d [Hz]\n',fp_out_result);
fT_result=fT_function(gm1,Cout_result);
fprintf('unity gain frequency fT=%d [Hz]\n',fT_result);
db_result=db_function(Av1_result);
fprintf('dB=%d [dB]\n',db_result);

function C1_result=C1_function(Cgs1)
C1_result=Cgs1;
end
function C2_result=C2_function(Cgd1,Cdb1,Cgs2,Csb2)
```

```
C2_result=Cgd1+Cdb1+Cgs2+Csb2;
end
function C3_result=C3_function(Cgs3,Cgd4,Csb3,Cdb4)
C3_result=Cgs3+Cgd4+Csb3+Cdb4;
end
function Cout_result=Cout_function(Cgd2,Cgd3,Cdb2,Cdb3,CL)
Cout_result=Cgd2+Cgd3+Cdb2+Cdb3+CL;
end
function Rpcascode_result=Rpcascode_function(gm3,gds3,gds4)
Rpcascode_result=gm3/(gds3*gds4);
end
function Rncascode_result=Rncascode_function(gm2,gds2,gds1)
Rncascode_result=gm2/(gds2*gds1);
end
function Rout_result=Rout_function(Rpcascode_result,Rncascode_result)
Rout_result=(Rncascode_result*Rpcascode_result)/(Rncascode_result+Rpcascode_result);
end
function Av1_result=Av1_function(gm1,Rout_result)
Av1_result=-gm1*Rout_result;
end
function Av2_result=Av2_function(gm1,gm2)
Av2_result=-gm1/gm2;
end
function Av3_result=Av3_function(gm4,gm3)
Av3_result=-gm4/gm3;
end
function fp_out_result=fp_out_function(Rout_result,Cout_result)
fp_out_result=(1/(2*pi*Rout_result*Cout_result));
end
function fT_result=fT_function(gm1,Cout_result)
fT_result=(1/(2*pi))*(gm1/Cout_result);
end
function db_result=db_function(Av1_result)
db_result=20*log10(Av1_result);
end
Result:
C1=6.301010e-14 [F]
C2=1.663449e-13 [F]
C3=3.506942e-13 [F]
Cout=6.001661e-13 [F]
Rpcascode=6.398513e+07 [Ohms]
Rncascode=1.967186e+08 [Ohms]
Rout=4.828111e+07 [Ohms]
Av1=-2.535505e+04 [V/V]
node 1 Av2=-9.859022e-01 [V/V]
node 3 Av3=-1.000015e+00 [V/V]
pole fp_out=5.492517e+03 [Hz]
unity gain frequency fT=1.392630e+08 [Hz]
dB=8.808129e+01 [dB]
```

Code 23. Matlab calculation for output resistance of mirrored cascode

```
gds12=4.2435*10^-6;
gds13=9.4612*10^-6;
gm13=571.7416*10^-6;
gds6=3.7346*10^-6;
gds7=2.6893*10^-6;
gm6=939.8841*10^-6;


rout_result=rout_function(gds12,gds13,gm6,gds6,gds7,gm13);
fprintf('The output resistance of mirrored cascode single stage OTA rout=%d
[Ohm]\n',rout_result);

function rout_result=rout_function(gds12,gds13,gm6,gds6,gds7,gm13)

rout_result=((1/gds12)*gm13*(1/gds13)*(1/gds7)*gm6*(1/gds6))/((1/gds12)*gm13*(1/gds13)+(1
/gds7)*gm6*(1/gds6));
end
```

```
Result:
The output resistance of mirrored cascode single stage OTA rout=1.235980e+07 [Ohm]
```

APPENDIX C

Netlist 1. Schematic NMOS

```
* SPICE export by:  S-Edit 2019.2.0
* Export time:     Sun Mar 12 16:43:44 2023
* Design path:     C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\lib.defs
* Library:         DESIGNS
* Cell:           Cell_PMOS
* Testbench:       Spice
* View:           schematic
* Export as:       top-level cell
* Export mode:     hierarchical
* Exclude empty:   yes
* Exclude .model:   no
* Exclude .hdl:    no
* Exclude .end:    no
* Expand paths:    yes
* Wrap lines:      no
* Exclude simulator commands:  no
* Exclude global pins:        no
* Exclude instance locations:  no
* Control property name(s):    SPICE
********* Simulation Settings - General Section *********
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
********* Simulation Settings - Parameters *********
.param VGS = 3.3
.param VDS = 3.3
***** Top Level *****
MM1 D G Gnd Gnd MODN W=3.5u L=350n AS=3.15p PS=8.8u AD=3.15p PD=8.8u $ $x=4500 $y=4100
$w=400 $h=600
VDS D Gnd  DC VDS $ $x=6100 $y=4100 $w=400 $h=600
VGS G Gnd  DC VGS $ $x=3800 $y=3800 $w=400 $h=600
.PLOT    I(MM1,D) $ $x=6900 $y=4800 $w=2000 $h=400
.PLOT    gm(MM1) $ $x=6150 $y=2650 $w=3300 $h=300
********* Simulation Settings - Analysis Section *********
.op
.dc VDS 0v 3.3v 0.01 SWEEP VGS 0v 3.3v 0.6
********* Simulation Settings - Additional SPICE Commands *********
.dc lin param VGS 0v 3.3v 0.001
.end
```

Netlist 2. Layout NMOS

```
*******************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Sun Mar 12 12:52:56 2023
* L-Edit Version:              L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:               C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
```

```
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                    cell_NMOS
* Write Flat:                   NO
********************************************************************************
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
.temp 25
**************************************
.param VDS=3.3
.param VGS=3.3
**************************************
M1 D G GND GND MODN l=3.5e-07 w=3.5e-06 ad=3.15e-12 as=3.15e-12 pd=8.8e-06 ps=8.8e-06  $ (13.825
18.688 14.175 22.188)
**************************************
VDS D GND VDS
VGS G GND VGS
**************************************
.dc lin param VDS 0v 3.3v 0.1v sweep VGS 0v 3.3v 0.6v
.dc lin param VGS 0v 3.3v 0.001
**************************************
.print dc i(M1,D)
.print dc gm(M1)
**************************************
* Top level device count
* M(NMOS25)                  1
* Number of devices:         1
* Number of nodes:  3
```

Netlist 3. Schematic PMOS

```
* SPICE export by:  S-Edit 2019.2.0
* Export time:     Wed Mar 29 11:50:52 2023
* Design path:     C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\lib.defs
* Library:         DESIGNS
* Cell:           Cell_NMOS
* Testbench:       Spice
* View:           schematic
* Export as:       top-level cell
* Export mode:     hierarchical
* Exclude empty:   yes
* Exclude .model:   no
* Exclude .hdl:    no
* Exclude .end:    no
* Expand paths:    yes
* Wrap lines:      no
* Exclude simulator commands:  no
* Exclude global pins:        no
* Exclude instance locations:  no
* Control property name(s):    SPICE
********* Simulation Settings - General Section *********
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
********* Simulation Settings - Parameters *********
.param VSG = 3.3
.param VSD = 3.3
.param VDD = 3.3
***** Top Level *****
```

```
MM1 D G Vdd Vdd MODP W=3.5u L=350n AS=3.15p PS=8.8u AD=3.15p PD=8.8u $ $x=4500 $y=4500
$w=400 $h=600
VSD Vdd D  DC VSD $ $x=5900 $y=4500 $w=400 $h=600
VSG Vdd G  DC VSG $ $x=4000 $y=4800 $w=400 $h=600
VVDD Vdd Gnd  DC VDD $ $x=6700 $y=4500 $w=400 $h=600
.PLOT    I(MM1,D) $ $x=3700 $y=3700 $w=2000 $h=400 $r=180
.PLOT    gm(MM1) $ $x=12750 $y=4950 $w=3300 $h=300
********* Simulation Settings - Analysis Section *********
.op
.dc VSD 0v 3.3v 0.1 SWEEP VSG 0v 3.3v 0.6
********* Simulation Settings - Additional SPICE Commands *********
.dc lin param VSG 0v 3.3v 0.001
.end
```

Netlist 4. Layout PMOS

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Sun Mar 12 13:26:27 2023
* L-Edit Version:              L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:               C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                  cell_PMOS
* Write Flat:                 NO
********************************************************************************
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\SPICELEVEL49.lib"
.temp 25
**************************************
.param VSD=3.3
.param VSG=3.3
.param VDD=3.3
**************************************
M1 D G VDD VDD MODP l=3.5e-07 w=3.5e-06 ad=3.15e-12 as=3.15e-12 pd=8.8e-06 ps=8.8e-06  $ (35.84
13.123 36.19 16.623)
**************************************
VSD VDD D  DC VSD
VSG VDD G VSG DC VSG
VSD1 VDD GND DC VDD
**************************************
.dc lin param VSD 0v 3.3v 0.1 sweep lin param VSG 0v 3.3v 0.6
.dc lin param VSG 0v 3.3v 0.001
**************************************
.print dc i(M1,D)
.print dc gm(M1)
**************************************
* Top level device count
* M(PMOS25)                   1
* Number of devices:          1
* Number of nodes:  3
```

Netlist 5. Layout diode CMOS

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Mon Mar 13 11:46:38 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_DIODE_CONNECTED_CMOS
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\SPICE_MODELS\LEVEL1\SPICELEVEL1_Tech_0.5um.lib"
********* Simulation Settings - Parameters *********
.param VDS1 = 1.2V
.param VDS2 = 1.2V
.param VDS3 = 1.2V
.param VSD4 = 1.2V
.param VSD5 = 1.2V
.param VSD6 = 1.2V
****************************************
M1 G1 G1 GND1 GND1 MODN l=2e-06 w=5e-06 ad=4.5e-12 as=4.5e-12 pd=1.18e-05 ps=1.18e-05  $ (31.97
21.943 33.97 26.943)
M2 G2 G2 GND2 GND2 MODN l=1e-06 w=1e-05 ad=9e-12 as=9e-12 pd=2.18e-05 ps=2.18e-05  $ (33.73 -4.16
34.73 5.84)
M3 G3 G3 GND3 GND3 MODN l=2e-06 w=2e-05 ad=1.8e-11 as=1.8e-11 pd=4.18e-05 ps=4.18e-05  $ (48.32
14.443 50.32 34.443)
M4 GND4 GND4 S4 S4 MODP l=2e-06 w=5e-06 ad=4.5e-12 as=4.5e-12 pd=1.18e-05 ps=1.18e-05  $ (71.97
21.943 73.97 26.943)
M5 GND5 GND5 S5 S5 MODP l=1e-06 w=1e-05 ad=9e-12 as=9e-12 pd=2.18e-05 ps=2.18e-05  $ (73.73 -4.16
74.73 5.84)
M6 GND6 GND6 S6 S6 MODP l=2e-06 w=2e-05 ad=1.8e-11 as=1.8e-11 pd=4.18e-05 ps=4.18e-05  $ (88.32
14.443 90.32 34.443)
****************************************
VDS1 G1 GND1 DC VDS1
VDS2 G2 GND2 DC VDS2
VDS3 G3 GND3 DC VDS3
VSD4 S4 GND4 DC VSD4
VSD5 S5 GND5 DC VSD5
VSD6 S6 GND6 DC VSD6
****************************************
.op
****************************************
* Top level device count
* M(NMOS25)                  3
* M(PMOS25)                  3
* Number of devices:         6
* Number of nodes:  11
```

Netlist 6. Layout resistor

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Mon Mar 13 14:14:59 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_resitance
* Write Flat:               NO
********************************************************************************
R1 5 6  r=308.824  $ (49.695 -96.465 74.695 -96.125)
****************************************
* Top level device count
* R()            3
* Number of devices:        3
* Number of nodes:  6
```

Netlist 7. Seprentine resistor

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Wed Mar 29 13:25:48 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_resitance
* Write Flat:               NO
********************************************************************************
R1 1 2  r=995.303  $ (-20.765 -40.248 -5.788 -11.248)
****************************************
* Top level device count
* R()            3
* Number of devices:        3
* Number of nodes:  6
```

Netlist 8. Layout capacitor

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Wed Mar 29 13:30:10 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
```

```
* TDB File Name:            C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_capacitor_2pF
* Write Flat:               NO
********************************************************************************
C1 1 2  c=2.04619e-12  $ (-4.5 14.75 21.5 35.75)
**************************************
* Top level device count
* C()            1
* Number of devices:        1
* Number of nodes:  2
```

Netlist 9. Layout push-pull inverter

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Tue Mar 14 19:08:20 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:            C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_INVERTER
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\tsmc035.lib"
**************************************
.param Vin = 0
.param VDD = 0
**************************************
C1 OUT GND  c=5.01662e-13  $ (22.945 43.538 33.445 59.038)
M1 OUT In GND GND MODN l=7e-07 w=7e-06 ad=6.3e-12 as=6.3e-12 pd=1.58e-05 ps=1.58e-05  $ (4.62
56.613 5.32 63.613)
M2 OUT In VDD VDD MODP l=7e-07 w=7e-06 ad=6.3e-12 as=6.3e-12 pd=1.58e-05 ps=1.58e-05  $ (4.62
66.163 5.32 73.163)
VV1 VDD GND DC 3.3
VV2 In N_1 DC Vin
VV3 N_1 N_2 DC 0 AC 1 0
VV4 N_2 GND SIN(0 20m 10k 0 0 0)
**************************************
.PLOT V(In)
.PLOT V(OUT)
.PLOT AC Vdb(OUT)
.PLOT AC Vp(OUT)
.PLOT I(M1,OUT)
**************************************
.MEASURE AC Av_dB MAX vdb(OUT)
.MEASURE AC PM FIND 'vp(OUT)' WHEN vdb(OUT)=0
.MEASURE AC ft WHEN Vdb(OUT)=0
```

```
.MEASURE AC minus_threedb_pole_MaxGain MAX vdb(OUT) PRINT 0
.MEASURE AC minus_threedb_pole WHEN Vdb(OUT)='minus_threedb_pole_MaxGain-3'
****************************************
.tran 0.01u 5m
.dc Vin 0v 3.3v 0.0001
.dc Vin 0v 3.3v 0.001 sweep VV1 0.66v 3.3v 0.66
.ac DEC 10 1 1G
.end
****************************************
* Top level device count
* C()            1
* M(NMOS25)              1
* M(PMOS25)              1
* Number of devices:     3
* Number of nodes:  4
```

Netlist 10. Layout inverter with active load

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Sat Mar 11 01:59:29 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_INVERTER_WITH_ACTIVE_LOAD
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\tsmc035.lib"
****************************************
C1 OUT GND  c=5.01662e-13  $ (43.36 25.375 53.86 40.875)
M1 GND IN OUT GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $
(22.575 10.325 23.275 45.325)
M2 OUT IBIAS VDD VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $
(22.225 49.775 23.625 77.775)
M3 VDD IBIAS IBIAS VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $
(22.225 81.375 23.625 109.375)
****************************************
VV1 IN N_1 DC 604.8412m
VVDD VDD GND DC 3.3
VV2 N_1 N_2 DC 0 AC 1 0
VV3 N_2 GND SIN(0 2.5m 10k 0 0 0)
IBIAS IBIAS GND DC 30u
****************************************
.PLOT V(IN)
.PLOT V(OUT)
.PLOT AC Vdb(OUT)
.PLOT AC Vp(OUT)
****************************************
.op
.tran 0.01u 5m start=0
.ac DEC 10 1 1G
```

```
**************************************
.MEASURE AC Av_dB MAX vdb(OUT)
.MEASURE AC PM FIND 'vp(OUT)' WHEN vdb(OUT)=0
.MEASURE AC ft WHEN Vdb(OUT)=0
.MEASURE AC minus_threedb_pole_MaxGain MAX vdb(OUT) PRINT 0
.MEASURE AC minus_threedb_pole WHEN Vdb(OUT)='minus_threedb_pole_MaxGain-3'
```

Netlist 11. Layout cascode with active load

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Sat Mar 11 02:10:38 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_CASCODE_WITH_ACTIVE_LOAD
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\tsmc035.lib"
**************************************

C1 OUT GND  c=5.01662e-13  $ (-22.265 -178.535 -11.765 -163.035)
M1 1 IN GND GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $ (-50.925
-193.585 -50.225 -158.585)
M2 OUT VB 1 GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $ (-43.05 -
193.585 -42.35 -158.585)
M3 OUT IBIAS VDD VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-
43.4 -154.135 -42 -126.135)
M4 VDD IBIAS IBIAS VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $
(-43.4 -122.535 -42 -94.535)
**************************************
VV1 IN N_1 DC 604.8412m
VV2 VB GND DC 1.3733
VVDD VDD GND DC 3.3
VV3 N_1 N_2 DC 0 AC 1 0
VV4 N_2 GND SIN(0 2.5m 10k 0 0 0)
IBIAS IBIAS GND DC 30u
**************************************
.PLOT V(IN)
.PLOT V(OUT)
.PLOT AC Vdb(OUT)
.PLOT AC Vp(OUT)
**************************************
.op
.tran 0.01u 5m start=0
.ac DEC 10 1 1G
**************************************
.MEASURE AC Av_dB MAX vdb(OUT)
.MEASURE AC PM FIND 'vp(OUT)' WHEN vdb(OUT)=0
.MEASURE AC ft WHEN Vdb(OUT)=0
.MEASURE AC minus_threedb_pole_MaxGain MAX vdb(OUT) PRINT 0
```

```
.MEASURE AC minus_threedb_pole WHEN Vdb(OUT)='minus_threedb_pole_MaxGain-3'
```

Netlist 12. Layout cascode with cascode load

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Sat Mar 11 02:25:59 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_CASCODE_WITH_CASCODE_LOAD
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\tsmc035.lib"
**************************************
C1 OUT GND  c=5.01662e-13  $ (-2081.39 91954.3 -2070.89 91969.8)
M1 1 IN GND GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $ (-
2110.05 91939.2 -2109.35 91974.2)
M2 OUT VB1 1 GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $ (-
2102.17 91939.2 -2101.47 91974.2)
M3 2 IBIAS VDD VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-
2102.52 91980.7 -2101.12 92008.7)
M4 VDD IBIAS IBIAS VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $
(-2102.52 92012.3 -2101.12 92040.3)
M5 OUT VB2 2 VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-
2093.27 91980.7 -2091.87 92008.7)
**************************************
VV1 IN N_1 DC 604.8412m
VV2 VB1 GND DC 1.3733
VV3 VB2 GND DC 1.2037
VVDD VDD GND DC 3.3
VV4 N_1 N_2 DC 0 AC 1 0
VV5 N_2 GND SIN(0 20u 1k 0 0 0)
IBIAS IBIAS GND DC 30u
**************************************
.PLOT V(IN)
.PLOT V(OUT)
.PLOT AC Vdb(OUT)
.PLOT AC Vp(OUT)
**************************************
.op
.tran 0.01u 5m start=0
.ac DEC 10 1 1G
**************************************
.MEASURE AC Av_dB MAX vdb(OUT)
.MEASURE AC PM FIND 'vp(OUT)' WHEN vdb(OUT)=0
.MEASURE AC ft WHEN Vdb(OUT)=0
.MEASURE AC minus_threedb_pole_MaxGain MAX vdb(OUT) PRINT 0
.MEASURE AC minus_threedb_pole WHEN Vdb(OUT)='minus_threedb_pole_MaxGain-3'
```

Netlist 13. Layout differential amplifier

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Wed Mar 15 16:13:18 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_DIFFERENTIAL_AMPLIFIER
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\tsmc035.lib"
**************************************
C1 OUT GND  c=5.01662e-13  $ (888.955 139.715 899.455 155.215)
M1 IBIAS IBIAS GND GND MODN l=7e-07 w=4.2e-05 ad=3.78e-11 as=3.78e-11 pd=8.58e-05 ps=8.58e-05  $
(862.355 71.17 863.055 113.17)
M2 2 IN2 1 GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $ (862.355
120.74 863.055 155.74)
M3 GND IBIAS 2 GND MODN l=7e-07 w=4.2e-05 ad=3.78e-11 as=3.78e-11 pd=8.58e-05 ps=8.58e-05  $
(870.355 71.17 871.055 113.17)
M4 OUT IN1 2 GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $
(870.355 120.74 871.055 155.74)
M5 1 1 VDD VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (860.23
165.64 861.63 193.64)
M6 VDD 1 OUT VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $
(870.43 165.64 871.83 193.64)
**************************************
VVDD VDD GND DC 3.3
VV1 IN1 N_1 DC 1.239
VV2 N_1 GND SIN(0 1m 1k 0 0 0)
VV4 IN2 N_3 DC 1.239
VV3 N_3 N_4 DC 0 AC 1 0
VV5 N_4 GND SIN(0 -1m 1k 0 0 0)
IBIAS VDD IBIAS DC 60u
**************************************
.PLOT V(IN1)
.PLOT V(IN2)
.PLOT V(OUT)
.PLOT AC Vdb(OUT)
.PLOT AC Vp(OUT)
**************************************
.op
.tran 0.01u 5m start=0
.ac DEC 10 1 1G
**************************************
.MEASURE AC Av_dB MAX vdb(OUT)
.MEASURE AC PM FIND 'vp(OUT)' WHEN vdb(OUT)=0
.MEASURE AC ft WHEN Vdb(OUT)=0
.MEASURE AC minus_threedb_pole_MaxGain MAX vdb(OUT) PRINT 0
.MEASURE AC minus_threedb_pole WHEN Vdb(OUT)='minus_threedb_pole_MaxGain-3'
```

Netlist 14. Layout single stage mirrored cascode OTA

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Fri Mar 17 10:48:05 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_MIRRORED_CASCODE_SINGLE_STAGE_OTA
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\tsmc035.lib"
**************************************
C1 OUT GND  c=2.09408e-12  $ (38.155 55.995 63.155 75.995)
M1 1 1 GND GND MODN l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-
31.885 33.275 -30.485 61.275)
M2 1 2 2 GND MODN l=7e-07 w=2.8e-05 ad=3.5e-11 as=3.5e-11 pd=5.85e-05 ps=5.85e-05  $ (-23.785
33.275 -23.085 61.275)
M3 4 IN1 3 GND MODN l=7e-07 w=3.5e-05 ad=3.15e-11 as=3.15e-11 pd=7.18e-05 ps=7.18e-05  $ (-15.56
26.275 -14.86 61.275)
M4 GND VB1 3 GND MODN l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-
11.16 -10.115 -9.76 17.885)
M5 3 IN2 5 GND MODN l=7e-07 w=3.5001e-05 ad=3.15009e-11 as=3.15009e-11 pd=7.1802e-05 ps=7.1802e-
05  $ (-8.36 26.274 -7.66 61.275)
M6 OUT 2 6 GND MODN l=7e-07 w=2.8e-05 ad=3.5e-11 as=3.5e-11 pd=5.85e-05 ps=5.85e-05  $ (-0.135
33.275 0.565 61.275)
M7 GND 1 6 GND MODN l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (7.265
33.275 8.665 61.275)
M8 7 VB 2 VDD MODP l=7e-07 w=2.8e-05 ad=3.5e-11 as=3.5e-11 pd=5.85e-05 ps=5.85e-05  $ (-38.06 74.555
-37.36 102.555)
M9 VDD 4 7 VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-29.21
74.555 -27.81 102.555)
M10 4 4 VDD VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-15.91
74.555 -14.51 102.555)
M11 VDD 5 5 VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (-8.71
74.555 -7.31 102.555)
M12 8 5 VDD VDD MODP l=1.4e-06 w=2.8e-05 ad=2.52e-11 as=2.52e-11 pd=5.78e-05 ps=5.78e-05  $ (4.59
74.555 5.99 102.555)
M13 OUT VB 8 VDD MODP l=7e-07 w=2.8e-05 ad=3.5e-11 as=3.5e-11 pd=5.85e-05 ps=5.85e-05  $ (14.14
74.555 14.84 102.555)
**************************************
VVD VDD GND DC 3.3
VV1 IN1 N_1 DC 1.485
VV2 N_1 N_2 DC 0 AC 1 0
VV3 N_2 GND SIN(0 0.1m 1k 0 0 0)
VV4 IN2 N_3 DC 1.485
VV5 N_3 GND SIN(0 -0.1m 1k 0 0 0)
VV6 VB GND 1.557
VV7 VB1 GND 821.5468m
**************************************
.PLOT V(IN1)
.PLOT (IN2)
```

```
.PLOT V(OUT)
.PLOT AC Vdb(OUT)
.PLOT AC Vp(OUT)
**************************************
.op
.tran 0.01u 5m start=0
.ac DEC 10 1 1G
**************************************
.MEASURE AC Av_dB MAX vdb(OUT)
.MEASURE AC PM FIND 'vp(OUT)' WHEN vdb(OUT)=0
.MEASURE AC ft WHEN Vdb(OUT)=0
.MEASURE AC minus_threedb_pole_MaxGain MAX vdb(OUT) PRINT 0
.MEASURE AC minus_threedb_pole WHEN Vdb(OUT)='minus_threedb_pole_MaxGain-3'
**************************************
```

Netlist 15. Layout two stage operational amplifier

```
********************************************************************************
* SPICE netlist generated by Tanner Verify's NetList Extractor
*
* Extract Date/Time: Wed Mar 15 18:55:56 2023
* L-Edit Version:            L-Edit Win64 2019.2.20190514.21:14:33
*
* Rule Set Name:
* TDB File Name:             C:\Users\nikit\Documents\TannerEDA\MY-
PROJETCS\THESIS\LAYOUTS\DESIGNS.tdb
* PX Command File:
* Command File:
        C:\Users\nikit\Documents\TannerEDA\TannerTools_v2019.2\Process\Generic_250nm\Rules\EXT\Ge
neric_250nm.ext
* Cell Name:                cell_TWO_STAGE_OP_AMP_0.35um
* Write Flat:               NO
********************************************************************************
.TEMP 25
.lib "C:\Users\nikit\Documents\TannerEDA\MY-PROJETCS\THESIS\LEVEL49\tsmc035.lib"
**************************************
C1 1 OUT  c=1.80408e-12  $ (50.185 395.205 75.185 415.205)
R1 2 1  r=308.824  $ (42.355 96.865 42.695 121.865)
M1 3 3 GND GND MODN l=1.1e-06 w=7e-05 ad=6.3e-11 as=6.3e-11 pd=0.0001418 ps=0.0001418  $ (15.88
22.926 16.98 92.926)
M2 2 3 GND GND MODN l=1.1e-06 w=7e-05 ad=6.3e-11 as=6.3e-11 pd=0.0001418 ps=0.0001418  $ (24.28
22.926 25.38 92.926)
M3 GND 2 OUT GND MODN l=1.1e-06 w=0.00028 ad=2.52e-10 as=2.52e-10 pd=0.0005618 ps=0.0005618  $
(89.755 98.426 90.855 378.426)
M4 4 IN1 3 VDD MODP l=7e-07 w=0.000245 ad=2.205e-10 as=2.205e-10 pd=0.0004918 ps=0.0004918  $
(16.08 103.476 16.78 348.476)
M5 4 IBIAS VDD VDD MODP l=9e-07 w=7.5001e-05 ad=6.75009e-11 as=6.75009e-11 pd=0.000151802
ps=0.000151802  $ (21.268 360.476 22.168 435.477)
M6 IBIAS IBIAS VDD VDD MODP l=9e-07 w=0.000225 ad=2.025e-10 as=2.025e-10 pd=0.0004518
ps=0.0004518  $ (21.268 448.695 22.168 673.695)
M7 2 IN2 4 VDD MODP l=7e-07 w=0.000245 ad=2.205e-10 as=2.205e-10 pd=0.0004918 ps=0.0004918  $
(24.48 103.526 25.18 348.526)
M8 VDD IBIAS OUT VDD MODP l=9e-07 w=0.00015 ad=1.35e-10 as=1.35e-10 pd=0.0003018 ps=0.0003018  $
(45.968 519.976 46.868 669.976)
**************************************
VVD VDD GND DC 3.3
VV1 IN1 N_1 DC 754.1228m
VV2 N_1 GND SIN(0 1m 10k 0 0 0)
VV3 IN2 N_2 DC 754.1228m
```

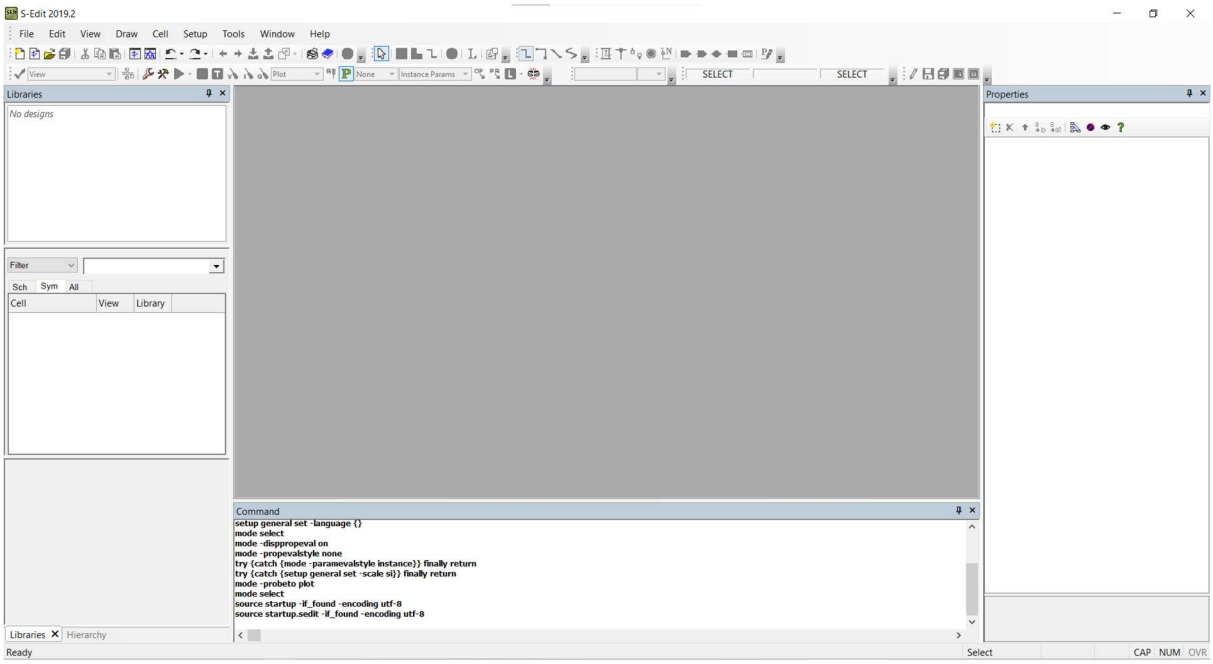
```
VV4 N_2 N_3 SIN(0 -1m 10k 0 0 0)
VV5 N_3 GND DC 0 AC 1 0
IBIAS IBIAS GND DC 300u
**************************************
.PLOT V(IN1)
.PLOT V(IN2)
.PLOT V(OUT)
.PLOT AC Vdb(OUT)
.PLOT AC Vp(OUT)
**************************************
.op
.tran 0.01u 5m start=0
.ac DEC 10 1 1G
**************************************
.MEASURE AC Av_dB MAX vdb(OUT)
.MEASURE AC PM FIND 'vp(OUT)' WHEN vdb(OUT)=0
.MEASURE AC ft WHEN Vdb(OUT)=0
.MEASURE AC minus_threedb_pole_MaxGain MAX vdb(OUT) PRINT 0
.MEASURE AC minus_threedb_pole WHEN Vdb(OUT)='minus_threedb_pole_MaxGain-3'
**************************************
```

APPENDIX D

S-edit:

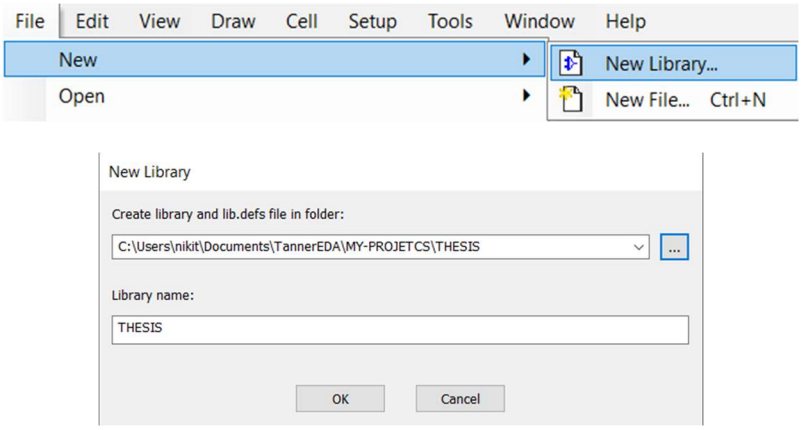
1. Interface of S-edit

Below we see the first window when we start the S-edit



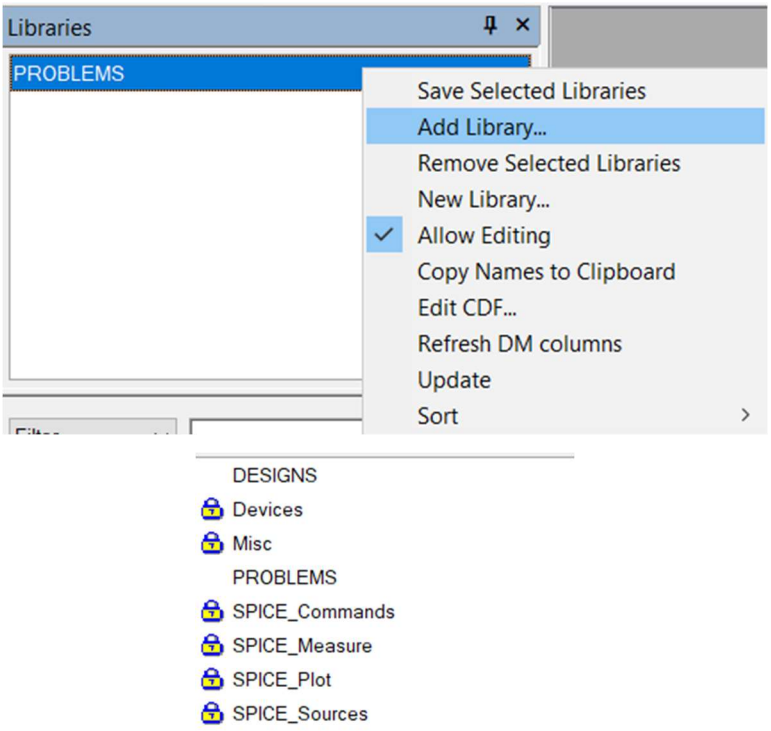
2. Create library file

Create a new library to have all the designs included to a file.



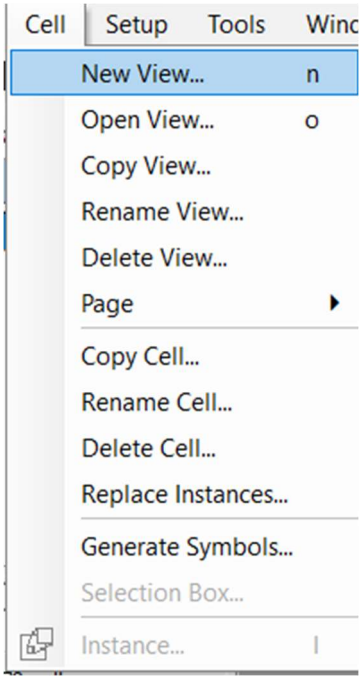
3. Add libraries to library file

Library files are important for the designer to have access to the components.



4. Create schematic view

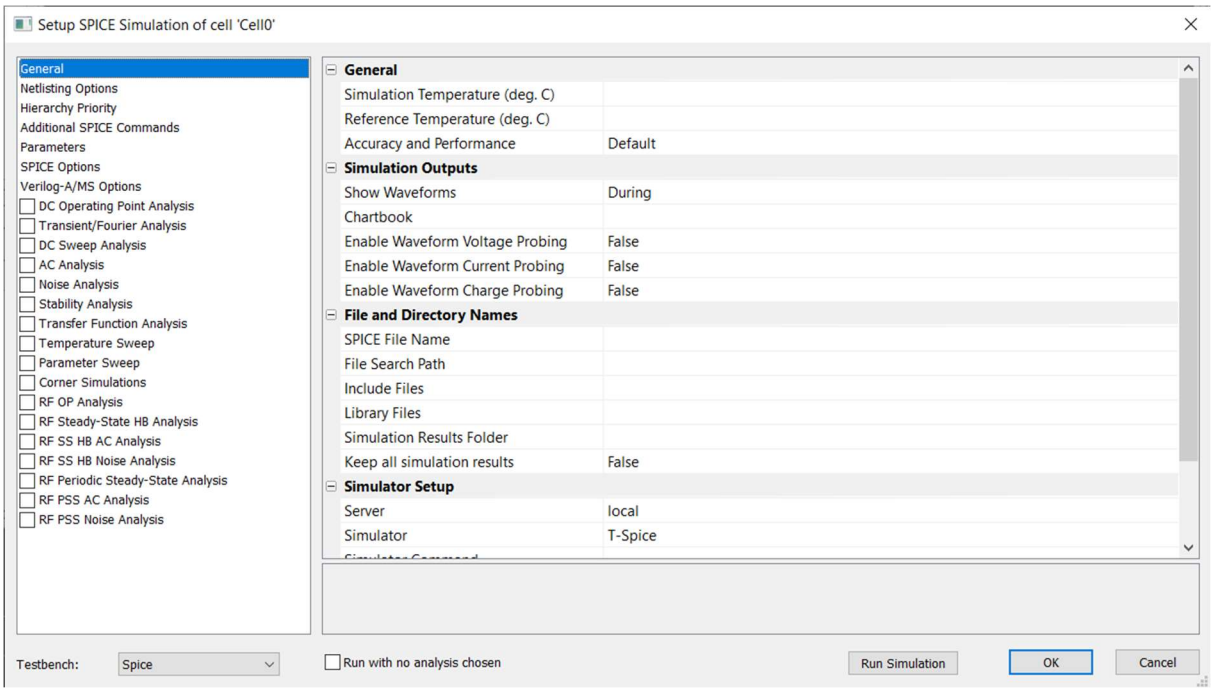
Creating the schematic view means that we create the schematic cell of the circuit.



5. Setup of spice simulation parameters

In the field *Library files* include the spice file.

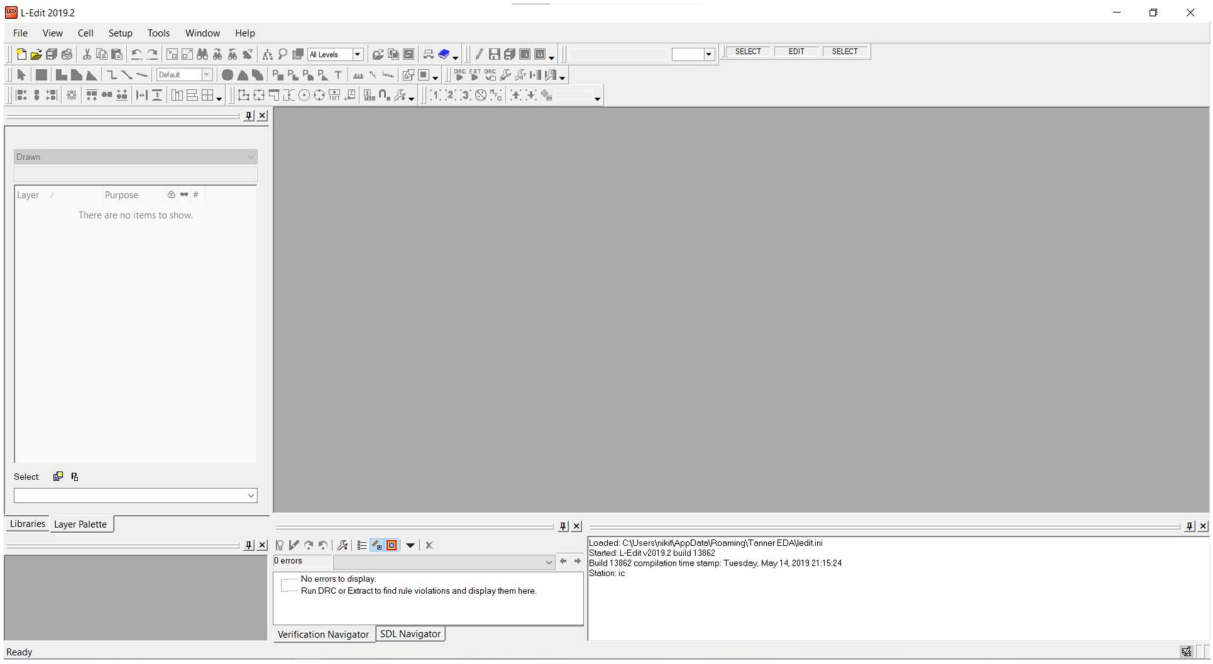
Select the analysis and define the appropriate parameters



L-edit:

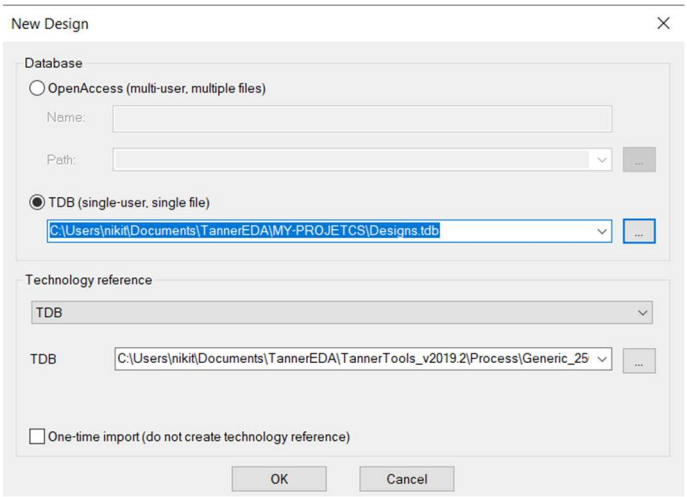
1. Interface of L-edit

Below we see the first window when we start the S-edit



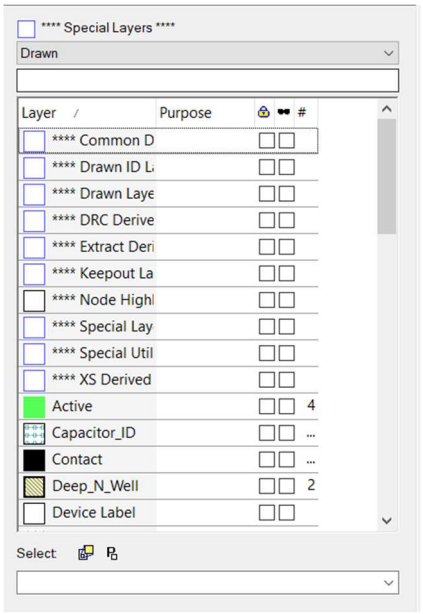
2. Create design file

Creating a new Design to have all the designs included to a file.



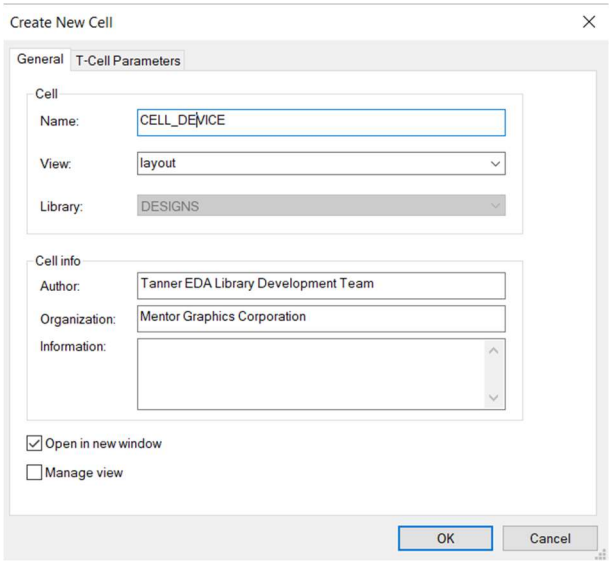
3. Layer pallete

Here we see all the layers that are useful for the designer.



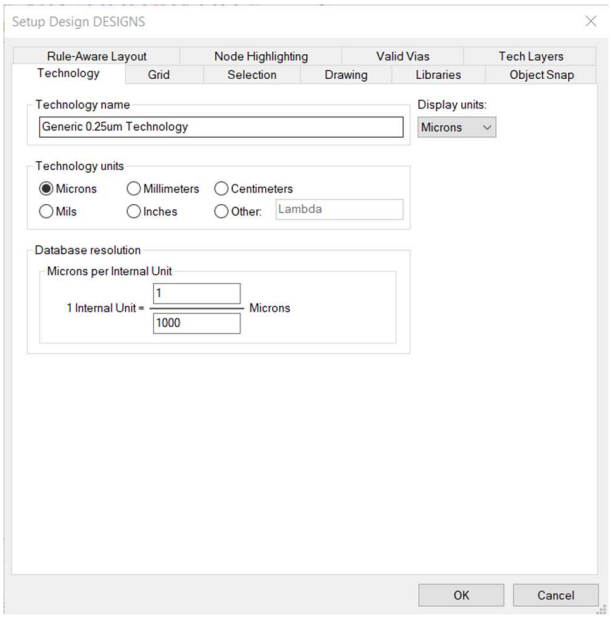
4. Create cell

Creating a cell means that we create the layout cell to design our circuit.



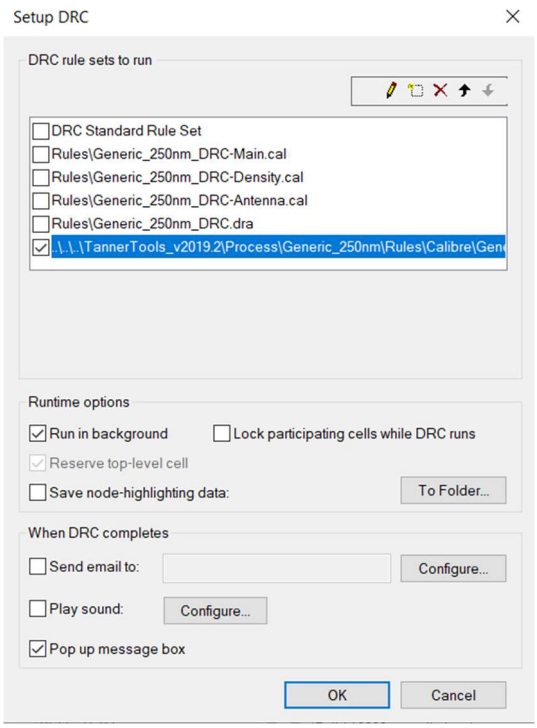
5. Setup design

In the setup menu we define the technology and all the necessary design parameters.



6. Setup DRC file

DRC (design rule checking) is important for the designer to check that the design fulfills all the necessary rules of the technology that uses



7. Setup extract file

Extract file is important because it creates the netlist of our design.