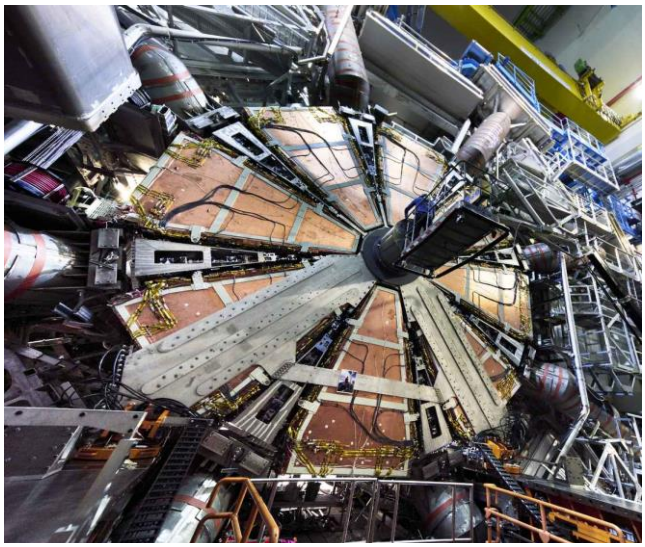
ΠΑΝΕΠΙΣΤΗΜΙΟ ΔΥΤΙΚΗΣ ΑΤΤΙΚΗΣ
ΣΧΟΛΗ ΜΗΧΑΝΙΚΩΝ
ΤΜΗΜΑ ΗΛΕΚΤΡΟΛΟΓΩΝ & ΗΛΕΚΤΡΟΝΙΚΩΝ ΜΗΧΑΝΙΚΩΝ

Πρόγραμμα Μεταπτυχιακών Σπουδών
«ΔΙΑΔΙΚΤΥΟ ΤΩΝ ΠΡΑΓΜΑΤΩΝ ΚΑΙ ΕΥΦΥΗ ΠΕΡΙΒΑΛΛΟΝΤΑ»

ΜΕΤΑΠΤΥΧΙΑΚΗ ΔΙΠΛΩΜΑΤΙΚΗ ΕΡΓΑΣΙΑ

Συστήματα ανάγνωσης και μεταφοράς δεδομένων στους ανιχνευτές του πειράματος ATLAS



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ΑΙΓΑΛΕΩ, Οκτώβριος 2022

UNIVERSITY OF WEST ATTICA

FACULTY OF ENGINEERING

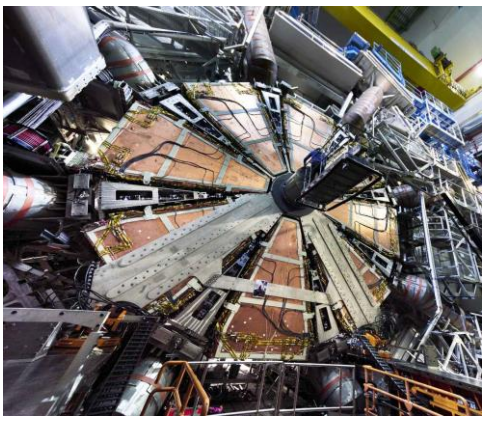
DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Master of Science in

"INTERNET of THINGS AND INTELLIGENT ENVIRONMENTS"

MSc Thesis

Readout and data transfer systems in the detectors of the ATLAS experiment



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ATHENS-EGALEO, October 2022

Η Διπλωματική Εργασία έγινε αποδεκτή και βαθμολογήθηκε από την εξής τριμελή επιτροπή:

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ΔΗΛΩΣΗ ΣΥΓΓΡΑΦΕΑ ΜΕΤΑΠΤΥΧΙΑΚΗΣ ΔΙΑΤΡΙΒΗΣ

Ο κάτωθι υπογεγραμμένος ΙΩΑΝΝΗΣ ΜΕΣΟΛΟΓΓΙΤΗΣ του ΠΑΝΤΕΛΗ με αριθμό μητρώου msciot18004, φοιτητής του Πανεπιστημίου Δυτικής Αττικής της Σχολής ΜΗΧΑΝΙΚΩΝ του Τμήματος ΗΛΕΚΤΡΟΛΟΓΩΝ ΚΑΙ ΗΛΕΚΤΡΟΝΙΚΩΝ ΜΗΧΑΝΙΚΩΝ,

δηλώνω υπεύθυνα ότι:

«Είμαι συγγραφέας αυτής της διπλωματικής εργασίας και ότι κάθε βοήθεια την οποία είχα για την προετοιμασία της είναι πλήρως αναγνωρισμένη και αναφέρεται στην εργασία. Επίσης, οι όποιες πηγές από τις οποίες έκανα χρήση δεδομένων, ιδεών ή λέξεων, είτε ακριβώς είτε παραφρασμένες, αναφέρονται στο σύνολό τους, με πλήρη αναφορά στους συγγραφείς, τον εκδοτικό οίκο ή το περιοδικό, συμπεριλαμβανομένων και των πηγών που ενδεχομένως χρησιμοποιήθηκαν από το διαδίκτυο. Επίσης, βεβαιώνω ότι αυτή η εργασία έχει συγγραφεί από μένα αποκλειστικά και αποτελεί προϊόν πνευματικής ιδιοκτησίας τόσο δικής μου, όσο και του Ιδρύματος.

Παράβαση της ανωτέρω ακαδημαϊκής μου ευθύνης αποτελεί ουσιώδη λόγο για την ανάκληση του διπλώματός μου».

Ο Δηλών

ΙΩΑΝΝΗΣ ΜΕΣΟΛΟΓΓΙΤΗΣ

Με βάση την αναμενόμενη αύξηση της φωτεινότητας του αναβαθμισμένου επιταχυντή LHC, το σύστημα ανιχνευτών "New Small Wheel (NSW)" αντικατέστησε τον εσωτερικότερο σταθμό ανίχνευσης στην εμπρόσθια περιοχή του φασματόμετρου μιονίων ATLAS. Το NSW διαθέτει δύο νέες τεχνολογίες ανιχνευτών: τους ανιχνευτές Micromegas (MM) και τους small strip Thin Gas Chambers (sTGC), που περιλαμβάνουν περισσότερα από 2 εκατομμύρια κανάλια ανάγνωσης. Ο μεγάλος αριθμός καναλιών ανάγνωσης, οι υψηλοί ρυθμοί δεδομένων και οι δύσκολες συνθήκες υπό τις οποίες θα λειτουργεί το NSW θέτουν σημαντικές προκλήσεις για το σύστημα σκανδαλισμού και συλλογής δεδομένων. Οι πλακέτες Level-1 Data Driver Card (L1DDC) αποτελούν μέρος των ηλεκτρονικών στοιχείων του ανιχνευτή NSW. Τρεις τύποι καρτών L1DDC είχαν παραχθεί μαζικά- δύο για την αλυσίδα ανάγνωσης των MM και των sTGC και ένας για την αλυσίδα ηλεκτρονικών σκανδαλισμού των sTGC. Για τον μαζικό έλεγχο όλων των καρτών L1DDC, αναπτύχθηκε μια πλήρως αυτοματοποιημένη διάταξη ελέγχου. Οι έλεγχοι των συνολικά 1184 καρτών L1DDC πραγματοποιήθηκαν: στο Πανεπιστήμιο Δυτικής Αττικής (ΠΑΔΑ), στο Εθνικό Καποδιστριακό Πανεπιστήμιο Αθηνών (ΕΚΠΑ), στο Εθνικό Κέντρο Επιστημονικών Ερευνών (ΕΚΕΦΕ Δημόκριτος) και στο CERN.

Εκτός από την ανάπτυξη της διάταξης ελέγχου των L1DDCs και την αξιολόγηση της απόδοσης και την αποσφαλμάτωση των L1DDCs, σχεδιάστηκαν και δοκιμάστηκαν διάφορες πλακέτες εκτός του ανιχνευτή για την αντιμετώπιση διαφόρων προβλημάτων των ηλεκτρονικών συστημάτων NSW που προέκυψαν κατά την ενσωμάτωσή τους στον ανιχνευτή. Το πιο κρίσιμο ήταν τα σοβαρά προβλήματα θορύβου που έθεσαν σε κίνδυνο την έγκαιρη εγκατάσταση του NSW στον ανιχνευτή ATLAS, δεδομένης της εκκίνησης του LHC. Διερευνήθηκαν όλες οι πιθανές πηγές θορύβου και πραγματοποιήθηκαν οι κατάλληλες επισκευές. Η κύρια πηγή θορύβου εντοπίστηκε να είναι τα τροφοδοτικά που τροφοδοτούν όλα τα ηλεκτρονικά του ανιχνευτή. Κατα συνέπεια σχεδιάστηκε και υλοποιήθηκε ένα φίλτρο σε μια πλακέτα που τοποθετήθηκε στο εσωτερικό των τροφοδοτικών ICS, μειώνοντας το θόρυβο σε αποδεκτά επίπεδα. Οι πλακέτες αυτες (128+) ειναι οι πρώτες που φέρουν το λογότυπο UNIWA, και εγκαταστάθηκαν στον ανιχνευτή NSW (Side-C) και στα εφεδρικά ICS.

ΛΕΞΕΙΣ-ΚΛΕΙΔΙΑ: CERN, LHC, Πείραμα ATLAS, New Small Wheel (NSW), Ανιχνευτές Micromegas, Ανιχνευτές sTGC, L1DDC, FPGA, Clock Distribution board.

Abstract

To benefit from the expected increase in luminosity of the upgraded LHC accelerator, the detector system "New Small Wheel (NSW)" replaced the innermost detection station in the forward region of the ATLAS Muon Spectrometer. NSW features two new detector technologies; the resistive Micromegas detectors (MM) and the small strip Thin Gap Chambers (sTGC), comprising more than 2 million readout channels. The large number of readout channels, the high data rates, and the harsh conditions under which the NSW will operate pose significant challenges to its trigger and data acquisition system. The Level-1 Data Driver Card (L1DDC) boards are part of the NSW detector electronics. Three types of L1DDC boards had massively been produced; two for the readout chain of the MMs and sTGCs and one for the trigger electronics chain of the sTGCs. A fully automated testing setup has been developed to evaluate the performance of 1184 L1DDC boards that have been tested at four testing sites; at the University of West Attica (UNIWA), the National Kapodistrian University of Athens (NKUA), the National Centre for Scientific Research (NCSR Demokritos), and CERN.

Besides the L1DDCs testing setup development and the L1DDCs' performance evaluation and debugging, several off-detector boards have been designed and tested to address several problems of the NSW electronic systems that emerged during their integration on the detector. The most critical one was the severe noise problems which jeopardized the on-time installation of the NSW on the ATLAS detector given the LHC run startup. All possible noise sources have been investigated, and adequate repairs have been performed. The primary noise source has been identified to be the power supplies that power all the detector electronics. A filter has been designed and implemented on a mezzanine board hosted on the ICS power supplies' front panels reducing the noise to acceptable levels. The mezzanine boards (128) carrying the UNIWA logo have been installed on the NSW detector (Side-C) and the spare ICSes.

KEYWORDS: CERN, LHC, ATLAS Experiment, New Small Wheel (NSW), Micromegas, sTGC, L1DDC, FPGA, NSW Noise Investigation, Clock Distribution board.

Contents

The world's largest and highest-energy particle accelerator (Large Hadron Collider, LHC), which operates at the European Organization for Nuclear Research (CERN) on France–Switzerland border, will undergo two upgrades to increase its scientific potential for new scientific discoveries about the fundamental structure of the universe. The first upgrade (Phase I) was recently accomplished, while the second (Phase II) is foreseen for 2025-2027. The ATLAS detector, one of the main LHC experiments, must upgrade its detectors and electronics to maintain its current excellent performance in the resulting higher data rates and higher radiation environment than the previous LHC runs.

The most complex and challenging Phase I upgrade project of the ATLAS detector concerns the wheel-shaped detection stations, named Small Wheels (SW). Since the detector technologies used for the SW are not designed to handle efficiently high particle rates, and the triggering system used for detecting muon particles is expected to exceed the available bandwidth, the SW was recently replaced by a new detection station, the New Small Wheels (NSW). The NSW employs two detector technologies: the novel resistive Micromegas (MM) and the small strip Thin Gap Chambers (sTGC), aiming to improve triggering performance and provide precise spatial measurements.

The NSW Trigger and Data Acquisition (TDAQ) system's electronics that reside on the detectors have to meet stringent requirements, such as a large number of readout channels (2.1M for the MM and 331k for the sTGC) that must handle a time latency of 2.5μs (for Phase I) and be resistant to high radiation and magnetic field environment. To this end, new electronics were designed and manufactured consisting of custom-made boards using mainly radiation-tolerant ASICs. A series of continuously improved prototypes were designed and underwent rigorous testing before mass production.

The Level-1 Data Driver Card (L1DDC) is part of the Trigger and Data Acquisition system of the MM and sTGC detectors. The L1DDC resides on the detectors and handles the signals exchanged among the detector's Front-End electronics and the off-detector data acquisition network interface (Front-End LInk eXchange, FELIX) away from the ATLAS detector.

Three types of L1DDC boards have been designed and massively produced; two are part of the readout path of the sTGC detectors (TGC-L1DDC) and MM detectors sTGC-L1DDCs and one is part the of the sTGCs' trigger path (RIM-L1DDC).

This thesis made a significant contribution (firmware and software) to developing a fully automated testing setup to evaluate the performance of the L1DDC boards in the mass production phase. Four identical test stations have been implemented at the University of West Attica (UNIWA), the National Kapodistrian University of Athens (NKUA), the National Centre for Scientific Research (NCSR Demokritos), and CERN. In total, the performance of 572 sTGC-L1DDCs (522 production boards and 50 pre-production boards), 572 sTGC-L1DDCs (522 production boards and 50 pre-production boards) together with 40 RIM-L1DDCs has been evaluated, and in the majority of those boards, faults have been repaired. In total, 1056 L1DDC boards have been successfully mounted on the NSW (512 MM, 512 sTGC, and 32 RIM L1DDCs).

This master thesis was carried out under a contract awarded by the ATLAS collaboration for participating in the challenge of installing the NSW on the ATLAS detector under tight time constraints. Thus, in addition to the operation validation and debugging of the L1DDC boards in the pre-production and production phase, the author contributed to several projects to address

problems of the NSW electronic systems that emerged during their integration on the detector. Only the most important of those are included in this master thesis because their solution was critical to the on-time installation of the NSW.

In particular, several off-detector boards have been designed and tested; a Clock Distribution Board to distribute low jitter 160 MHz clocks to the RIM electronics through the RIM-L1DDC, an LVDS to TTL adapter Board for the validation of Micromegas detectors with cosmic rays, and a Differential Safety Mechanism board for protecting the Micromegas detectors against sudden increases in the static gauge pressure inside their volume. The Clock Distribution board development has been published in the scientific journal Journal of Instrumentation, Volume 17, May 2022, and the Differential Safety Mechanish in the Journal of Physics, Conference Series.

Moreover, this thesis contributed significantly to identifying and suppressing the severe noise problems that emerged while integrating the electronics into the Micromegas detectors. The most important result of the many months' tedious investigation of the possible noise source was identifying the primary noise source as the power supplies (ICS) that power all of the detector electronics. The solution to that critical issue was based on the design of a filter implemented on a mezzanine board hosted on the ICS power supplies' front panels. The mezzanine boards (128) carrying the UNIWA logo have been installed, on the Side-C NSW detector and the spares ICS, suppressing the noise.

The organization of the thesis is as follows:

The first two Chapters briefly describe the ATLAS experiment and NSW's detector technologies and electronics. In Chapter 3, the L1DDC board design from the prototype phase to the mass production is presented in detail. The development of the setup (hardware, firmware, and software) for evaluating the performance of the L1DDC in the production phase is presented in Chapter 4. The last Chapter 5 describes in detail the development of the off-detector boards mentioned above, the investigation, and all the actions taken to resolve the critical issue of noise that jeopardized the installation of the NSW.

Chapter 1 CERN and the ATLAS experiment

The European Center for Nuclear Research (CERN), based in Geneva, Switzerland, is the largest research laboratory in the world focused on particle physics research. CERN was established in 1954 by twelve member states, including the Hellenic Republic. Over almost seven decades, CERN grew in size, with more countries joining the collaboration.

1.1 The Large Hardon Collider

Between 1984 and 1989, a 26.7 km tunnel was constructed to be used by the Large Electron–Positron Collider (LEP [1] accelerator, which operated until 2000. Following LEP's end of life, the tunnel accommodates the Large Hadron Collider (LHC) [2], the world's largest and most powerful accelerator. Inside the tunnel are two beam pipes, each containing a beam of hadrons (protons or heavy ions). The beam pipes are in an extremely high vacuum ($10^{-13}\ atm$) in order to avoid collisions of the hadrons with air molecules. The LHC accelerates the two oppositely moving beams to speeds very close to the speed of light and collides them at defined points around its circumference, where large detectors are installed to detect the abundance of particles produced during the collisions. By measuring the characteristics of the particles produced, scientists are trying to draw conclusions that will increase knowledge about the existence and properties of the building blocks of matter and fundamental forces, as well as about the origins of the universe. As shown in Figure 1, the LHC is the last part of a chain of accelerators in which beams of protons are gradually accelerated before entering the LHC's large ring. Initially, protons released from a hydrogen source are accelerated in the LINear ACcelerator (LINAC2) and acquire energy of 50 MeV. They are then driven to the Proton Synchrotron Booster (PSB), where they are accelerated, and their energy is increased to 1.4 GeV. In the next two acceleration steps, they enter the Proton Synchrotron (PS) and Super Proton Synchrotron (SPS), where they acquire energy of 25 GeV and 450 GeV, respectively, and then enter the LHC ring. Finally, as mentioned earlier, at different points of LHC's circumference, four large underground caverns are constructed at varying depths up to 100m deep. These caverns accommodate the CERN's four main experiments, namely: the ATLAS [3], CMS [4], ALICE [5], and LHCb [6].

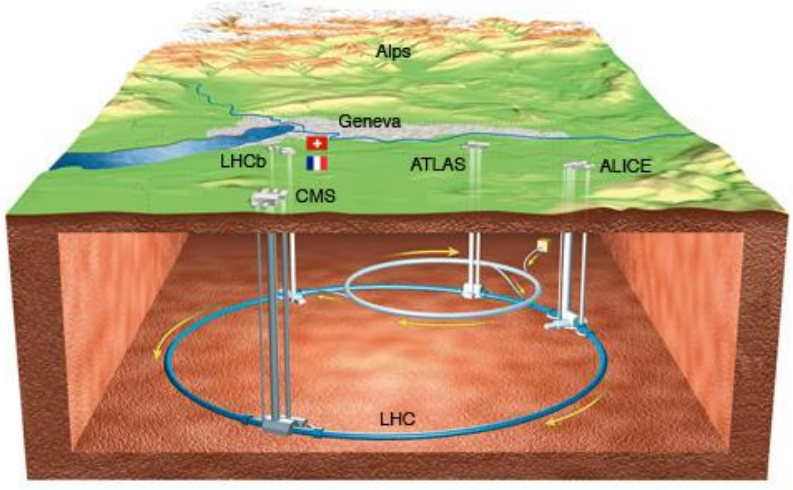


Figure 1: A graphical map of the LHC and the smaller accelerators SPS and PS. The locations of the four main experiments are also shown.

The LHC was first put into operation on 10 September 2008, and the first data started to be recorded and made available to scientists in 2010. During its first period of operation (Run1), which ended after three years (2013). Proton bunch collisions of 4 TeV energy each were achieved at that time. The most important discovery in this period was the discovery of the Higgs particle, the most sought-after particle in Elementary Particle Physics, linked to the mechanism by which particles acquired mass.

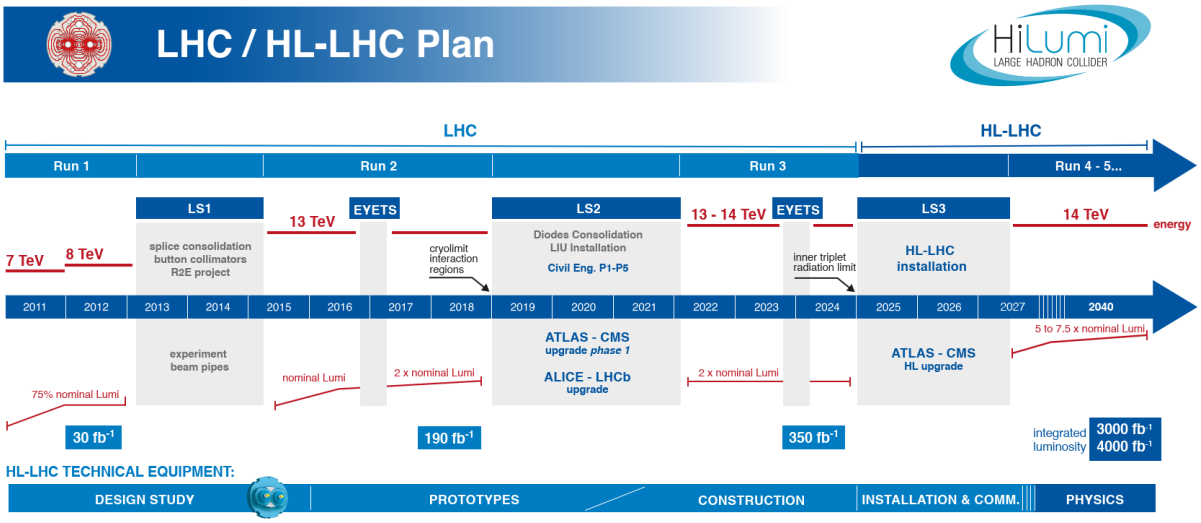


Figure 2: The LHC / HL-LHC schedule as of 2022.

As shown in Figure 2, two years (2013-2015) of repairs and upgrades (Long Shutdown 1, LS1) of both the accelerator and the experiments followed. In May 2015, the second period of operation of the accelerator (Run2) was inaugurated, which lasted until the end of 2018. From 2018 until march 2022, the first phase of the main experiment's upgrades was done in preparation for the High Luminosity-LHC (HL-LHC). The HL-LHC will achieve center-of-mass energy of 14 Tev and luminosity of $L = 5 - 7 \times 10^{34}\ cm^{-2}s^{-1}$, resulting in a large increase in the rate of events that the detectors and, subsequently, their electronic systems have to keep up with. According to the HL-LHC schedule, another shutdown period (LS3) between 2025–2027 will be done. During this shutdown, the HL-LHC installation and commissioning will occur. At the same time, the second phase of experiments' upgrades is scheduled to take place.

1.2 The ATLAS experiment

As mentioned in the previous section, one of the four main experiments installed at LHC's circumference is the ATLAS (A Toroidal LHC ApparatuS) experiment. The ATLAS detector is a general-purpose detector (like the CMS) in the sense that it is designed to cover as many interesting fields of research in particle physics as possible (unlike the other LHC experiments designed for specific studies). Those searches include precision measurements and research for the possible existence of new physics. The shape of the ATLAS detector is cylindrical, with a length of 45 m, a diameter of 25 m, and 7000 tons of mass (Figure 3). It consists of coaxial cylindrical detector subsystems around the beam axis (barrel region) and parallel detector plates on both sides of the barrel, perpendicular to the beam axis (end-caps region). Its subsystems are:

- The Magnet System

- The Inner Detector
- The Calorimeters
- The Muon Spectrometer
- The Trigger and Data Acquisition System (TDAQ)

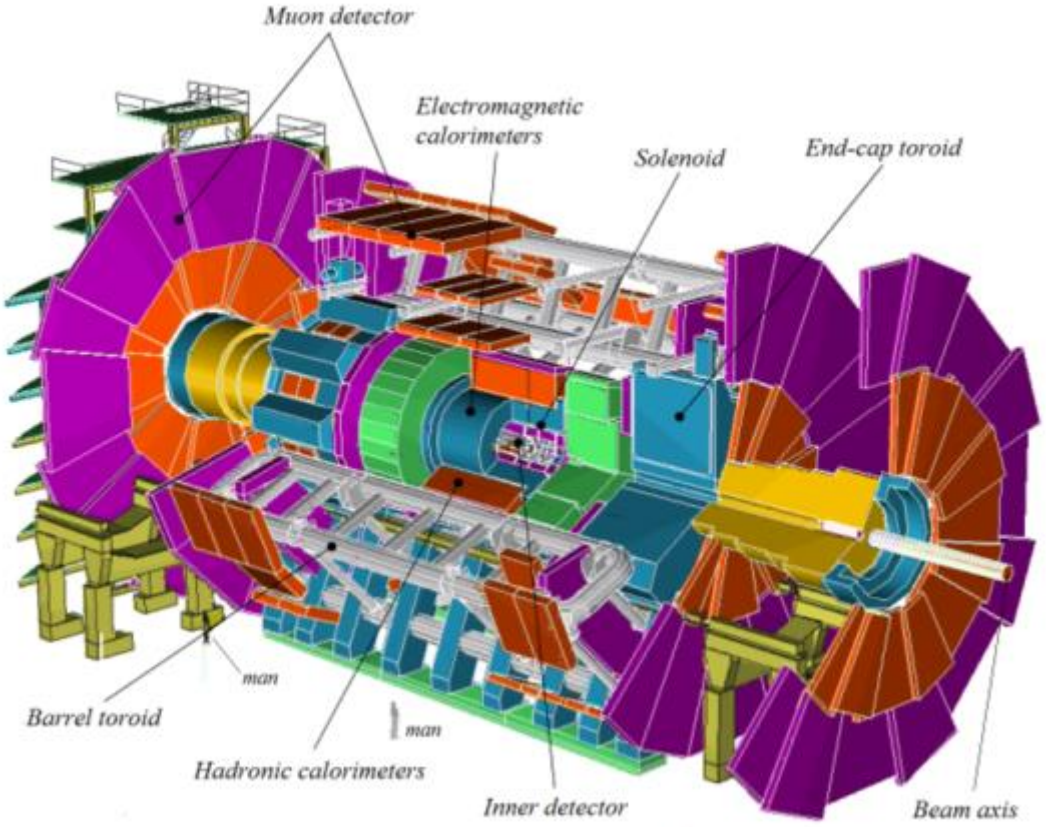


Figure 3: A graphical drawing of the ATLAS detector.

1.2.1 The Magnet System

The main feature of the ATLAS detector is the giant superconducting magnet system cooled by liquid helium at a temperature of 4.8 K. This system is designed to create the magnetic field needed to bend the trajectories of the generated particles in order to measure their momentum and determine their charge. The magnetic field is generated by four superconducting magnet systems: a central solenoid and three toroids.

The central solenoid [7] surrounds the Inner Detector (see below), has a length of 5.3 m, an external diameter of 2.4 m, and a weight of 5 tones. The solenoid uses superconducting wire (9km long), its operating current is 7.6kA, and it provides the Inner track Detector with a magnetic field along the beam axis of 2T intensity.

The toroidal magnet system is part of the muon spectrometer and provides an average magnetic field intensity of 4T. The magnetic field is generated by a) an air-cored barrel toroid [8] weighing 830 tones and 25 tones long, with 3 m length and 20.1 m outer diameters in the central region of ATLAS, and b) by two flat air-cored End Caps Toroids [9], one at each end of the cylindrical toroid, each weighing 240 tones, 5 m long, and 10.7 m outer diameter.

1.2.2 The Inner Detector

The Inner Detector (ID) [10] is the closest detector to the proton beam axis, covers the entire area around the collision point, and is contained in a 6.2 m long and 2.1 m diameter cylinder enclosed by the solenoid. The ID reconstructs (in the region near the beam axis) the trajectories of the generated charged particles to determine mainly their charge and momentum (from the curvature of their trajectories in the magnetic field). It consists of three types of sub-detectors of different technologies: The sub-detector closest to the beam axis is the Silicon Pixel detector [11] which is surrounded by the Semiconductor Tracker (SCT) [12], which in turn is surrounded by the Transition Radiation Tracker (TRT) [13]. The Pixel detector and SCT detect three and four space points (hits) of a candidate orbit, respectively, while the TRT detects 36 points, contributing significantly to improving the accuracy of momentum determination and particle identification.

The Pixel and SCT detectors use pixels and microstrips silicon technology, respectively, and their structure is three (four) coaxial barrels and four (nine) disks in each side region. The Pixel detector has 80 million pixels (readout channels), while the SCT consists of $60m^2$ silicon sensors and 6000 million readout channels to determine the momentum of each particle and the point at which it was created with high accuracy in the region near the collision point (where the particle density is very high).

The TRT detector uses gas detector technology and consists of 50000 gas-filled tubes of a tiny diameter (4mm) in the barrel region and 250000 in the two end-cap regions (18 detector disks on each side).

1.2.3 The Calorimeter

Outside the Inner Detector and the solenoid is the Calorimeter system. Calorimeters are detectors that measure the energy lost by particles as they pass through them and are designed to absorb all of their energy. Calorimeters can completely absorb and thus stop most of the known particles except for muons and neutrinos. The electromagnetic Calorimeters measure the energy of electrons, positrons, and photons, while the hadronic Calorimeters measure the energy of hadrons (particles made up of quarks, such as protons and neutrons). In addition, they can determine the location of the energy deposition, identify certain particles and assist in reconstructing the trajectory of the muons that pass through them.

The ATLAS Calorimeter system [14] uses Liquid Argon (LAr) [15] and Tile (TileCal) [16] Calorimeter technologies. It consists of the electromagnetic Calorimeter (two sections in the barrel region and two coaxial wheels), the hadronic Calorimeter in the barrel region (a cylinder consisting of the central barrel and two extended barrels), the hadronic Calorimeters in the end-cap regions (two wheels of radius 2. 09m) and the Forward Calorimeter (FCal). All Calorimeters use LAr technology, except the hadronic Calorimeter in the barrel area, which uses Tile technology.

The barrel region's electromagnetic and hadronic Calorimeter systems have an outer radius of 2.25 m and 4.23 m, respectively, while their total length is 6.65 m and 6.10 m, respectively, on either side of the proton beams interaction point.

1.2.4 The Muon Spectrometer

The Muon Spectrometer is used to precisely measure muons' momentum, one of the most interesting topics in physics carried out at the LHC.

Very high-energy muons deposit a small fraction of their energy in the Calorimeters; thus, measuring their energy using the Calorimeters alone is impossible. Therefore, the measurement

of their momentum must be based on tracking. However, tracking by using the Inner detector is not accurate enough to determine the momentum at high energies. For this reason, the ATLAS detector has a specialized high-precision trajectory measurement system, the Muon Spectrometer (MS) [17] (Figure 4), in combination with three large air-core toroids. The MS encloses the Calorimeter sections by radially covering the space between ~4.5m and 11m from the interaction point and between 7m and 23m on either side of the interaction point and delineates the dimensions of the ATLAS detector.

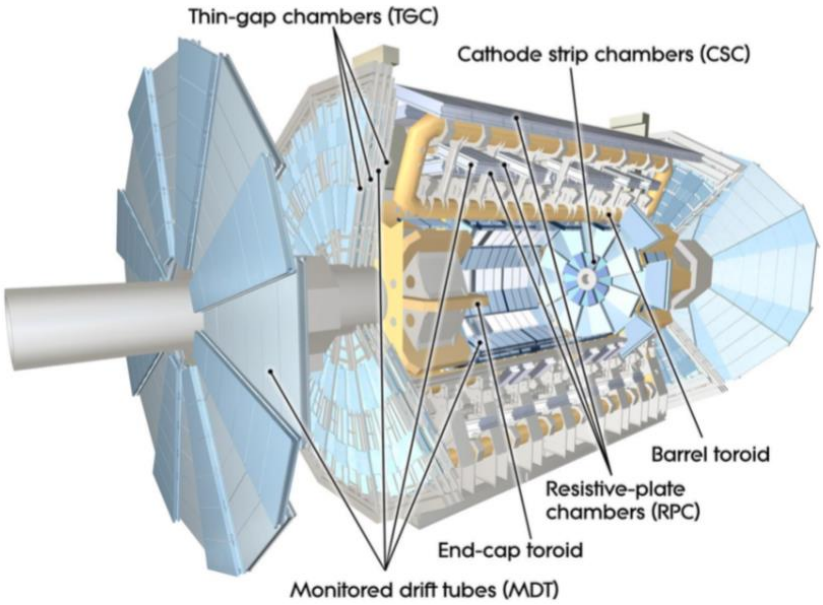


Figure 4: Graphical drawing of ATLAS detector, indicating the muon spectrometer's sub-detectors.

The muons' momentum is extracted from the curvature of their trajectories due to the magnetic field (0.4T and 1T intensity in the barrel and the end caps, respectively). The signals of the high-energy muons in the spectrometer have high purity because most of the other particles have already been absorbed in the calorimeter system.

As shown in Figure 4, the barrel region consists of three concentric cylindrical detector stations around the beam axis with radii of about 5m, 7.5m, and 10m, while the end cap regions consist of four detector stations (wheels) placed perpendicular to the beam axis at a distance of 7.4m, 10.8m, 14m and 21.5m from the collision point. Each spectrometer detector station is divided into eight sectors consisting of small and large detector modules that overlap to minimize the dead detection spots between sectors.

To accurately measure the high momentum of the muons, the spectrometer combines detectors of four different technologies:

The Cathode Strip Chambers (CSC) [18] detectors (in the end cap regions) and the Monitored Drift Tubes (MDT)[19] (in both the barrel region and end cap regions) are specialized for the accurate detection of hits' position coordinates used to reconstruct the trajectories of the muons passing through the spectrometer (tracking).

The Resistive Plate Chambers (RPC) [20] detectors in the barrel region and the Thin Gap Chambers (TGC) [21] in the end cap regions are specialized for muon triggering, i.e., for selecting from the set of detected hits those that may originate from real muons (triggering).

As shown in Figure 5, MDTs occupy most of the orbit detection detectors (99.5%), while CSCs occupy only a small area at the front end, where the particle flux is higher (due to their ability to operate efficiently in high-noise environments).

RPCs are fast-response detectors, while TGCs have a moderate response but operate more efficiently in the high-noise conditions prevalent in the end cap regions.

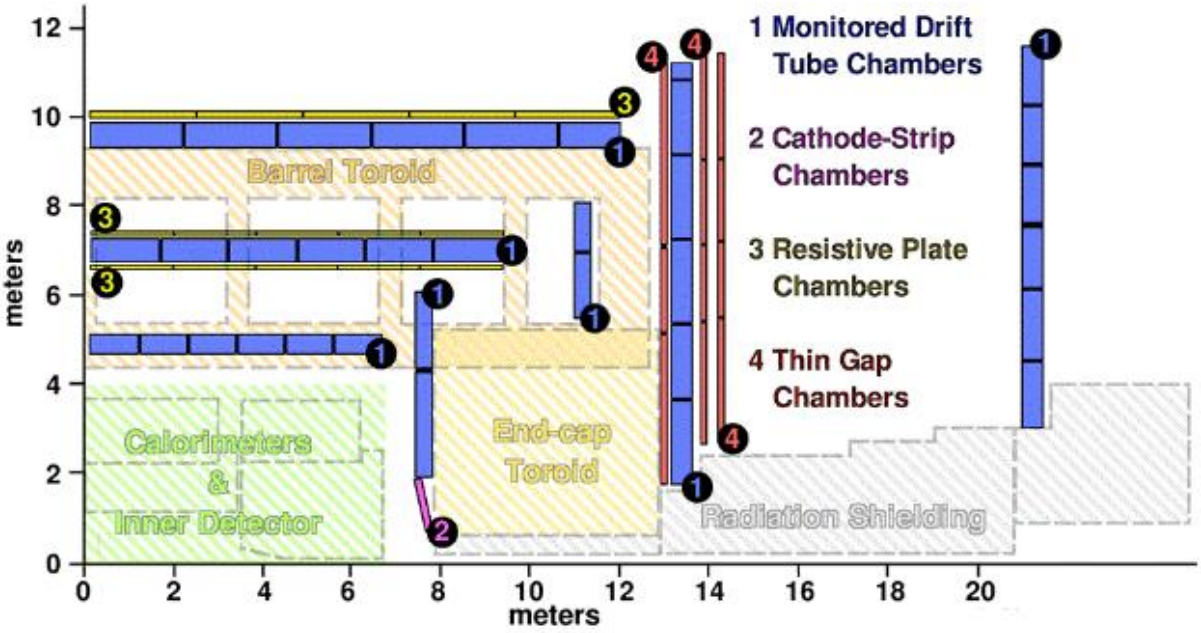


Figure 5: Cross-section view of the muon spectrometer. The beam is along the horizontal axis, and the origin corresponds to the beams' interaction point.

1.2.5 The Trigger and Data Acquisition System

In the LHC, the proton bunches collide every 25ns. The data collected by the detectors in each proton collision is about 1.6 Mb, so recording all the data in computer data storage is impossible. The Trigger System [22] of the ATLAS experiment is responsible for selecting (triggering) in real-time from the multitude of proton collisions, only those with interesting information for physics research. The Data Acquisition System (DAQ) transfers the data from the sub-detector Readout Drivers (RODs) at all stages up to their final storage in the experiment's storage system. During Run2, the triggering system (Figure 6) rejected events by a factor of 10^4, from the initial 40MHz rate of bunch collisions to just 1 kHz rate of events recorded for further analysis in non-real-time.

As shown in Figure 6, event rejection is achieved in two stages (levels): The Level-1 trigger (L1) is based on custom electronics having as input signals from the Calorimeters and a subset of the detectors of the muon spectrometer (the RPC and TGC sub-detectors). L1 determines detection regions with interesting information (Regions of Interest, RoI), such as high energy deposition in the Calorimeters or track segments of high transverse momentum muon candidates in the Muon Spectrometer. The L1 accept signal is distributed by the Timing, Trigger, and Control (TTC) system to the electronic readout systems of the sub-detectors and triggers their data readout and the RODs' processes. The data are then transferred to the Read-out System (ROS) [23] using the optical interface developed at CERN S-Link [24], where they are temporarily stored until the next level trigger signal is received. L1 triggering thereby reduces the maximum rate of the selected events to 100 kHz. The time (latency) after each collision for the Trigger system to analyze the sub-detector data, to decide that the event is interesting, and to forward the trigger signal to the electronic readout systems is 2.5 μs. At the same time, the data of the regions of interest are driven to the next stage of selection, the High-

Level Trigger (HLT). HLT is a computer farm where fast algorithms are executed that thoroughly study the data and further reduce the events' rate to 1kHz within an average time of 0.3s. The selected events are then driven to the experiment's computational storage system (Data Storage) for non-real-time reconstruction.

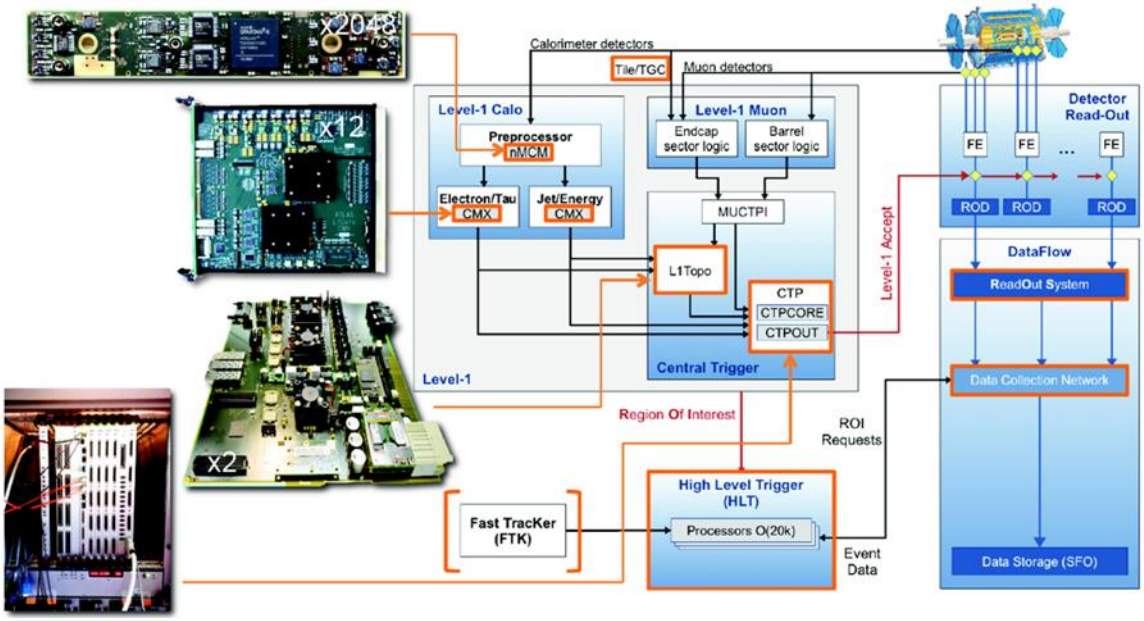


Figure 6: Block diagram of the ATLAS TDAQ system.

As mentioned above, the LHC upgrades will result, notably, in an increase in the number of proton collisions in each collision, high particle rate, a large amount of data that the electronic sub-detector readout systems have to handle, and aging of the silicon detectors due to radiation, necessitating an upgrade of the ATLAS detector. The first upgrade (Phase I upgrade) [25] of the detector took place during the 2018-2022 LHC shutdown period, while the second (Phase II upgrade) will take place in 2025-2027.

Specifically for the Muon Spectrometer, the first upgrade mainly concerned the Small Wheel (SW) detector system located at the end cap regions. The SW is located at a distance of 7m from the interaction point, and it is the closest to the interaction point detector system among the four detector wheels present in the end cap regions of the spectrometer (Figure 7).

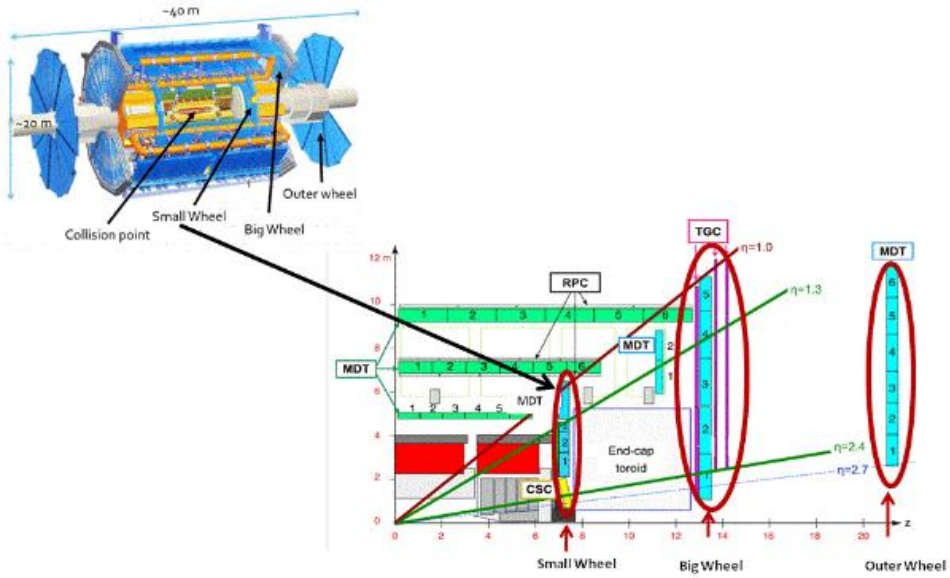


Figure 7: Top: The position of the Small Wheel. Bottom: The cross-section of the ATLAS muon spectrometer.

In the high luminosity conditions of the accelerator, there are mainly two important reasons that make it necessary to upgrade the SW detector disk:

A) The determination of first-level muon triggers in the spectrometer end cap regions is based on the reconstruction of muon trajectory segments and the determination of the proton collision point by the TGC detectors of the middle Big Wheel (BW) detector (since the vertical component of the momentum of a muon used to determine the trigger signal, is determined by the angle formed by the part of the track with the direction passing through the proton collision point). Studies have shown that these triggers are 90% false, i.e., they do not correspond to muons originating from the interaction point but to low-energy particles (mainly protons) produced in the material between the SW and BW detector. Those particles pass through the detector systems at an angle similar to real high-momentum muons. Therefore, with the large increase in the number of proton collisions due to the increase in LHC luminosity, there will be a large increase in spurious muon triggers in the end cap regions. It is estimated that the rate of muon triggers will exceed the 100kHz limit set for the whole ATLAS detector (20kHz for the muon spectrometer).

B) Concerning the SW detectors used mainly for muon tracking, significant degradation of their functionality is expected in terms of performance and accuracy of the measurement of the muon momentum. Since the determination of the muon momentum with high accuracy is highly dependent on the recorded signals in the SW detectors, this degradation will significantly affect the functionality of the whole ATLAS detector.

In order to address these problems, the SW detector system is replaced by the new New Small Wheel (NSW) system.

In the NSW detector system, to reduce the number of false triggers, the new triggering algorithm requires that the orbital segment of each muon reconstructed by the SW TGC detectors matches the corresponding segment reconstructed using the NSW detectors. For this, the NSW detectors must have a fast response, be able to determine the proton collision point under high particle flux conditions (15kHz/cm^2), and provide real-time (online) reconstructed track segments with an angular accuracy better than 1mrad, which is required to determine whether or not the track segment originates from the collision point. In addition, the NSW detectors must reconstruct the track segments in real-time within no more than 1 ms.

NSW has two detector technologies: small-strip Thin Gap Chambers (sTGC) and Resistive strip Micromegas (MM).

The sTGCs are used mainly as trigger detectors due to their excellent ability to determine the collision point and their very good (<1mrad) angular resolution in reconstructing parts of the tracks in real-time. In addition, the sTGCs can measure in non-real time (offline) the position coordinate in the radial direction with an accuracy of 100μm and the second position coordinate (used to combine the reconstruction of the muon trajectory by the Muon Spectrometer with that from the Inner Detector) with a lower accuracy (2-3mm).

The Resistive strip MicroMegas are primarily used as very accurate tracking detectors due to their excellent spatial resolution (<100μm), even at high particle rates. Besides that (due to their quite good time resolution), they can provide triggers that, combined with triggers from the Small Strip Thin Gas Chambers, can improve the level-1 triggering system. Both detectors belong to the category of gas-filled detector technology, whose operation is described in detail in the following two sections.

2.1 The Small-strip Thin Gas Chambers

The Thin Gap Chambers (TGC) detectors of the front regions of the Muon Spectrometer are relatively fast response detectors that perform well in the increased noise rate of that regions and measure the muon trajectories as a means to trigger the readout of the entire ATLAS detector data. As mentioned above, those detectors were appropriately modified (Small-strip Thin Gap Chambers, sTGC) to operate efficiently at high particle rates and can be used not only for fast triggering but also for reconstructing muon trajectories (tracking).

The sTGCs (like the TGCs) are a type of Multi-wire Proportional Chambers (MWPCs) [26], a detector technology proposed by Charpak in 1967-68, for which he received the Nobel Prize in 1992. This technology has been the basis for developing new, constantly evolving detectors with many applications, including experiments in elementary particle physics.

The MWPC detectors are gas-filled chambers delimited by two parallel flat surfaces (cathodes). Several wires at the same potential (anodes) are between them and equidistant from them. The wires are of tiny diameter and are arranged at equal and very small distances from each other. Usually, the distance between the plane of the anodes and cathodes is 3-4 times greater than the distance between the wires.

Their principle of operation is based on the ionization of the gas caused when a charged particle passes through the detector chamber. The ionization of the gas produces pairs of electrons and positive ions, which, under the influence of the electric field, drift toward the anodes and cathodes, respectively. If the voltage applied to the electrodes is such that the intensity of the electric field is high enough (of the order of 10^4-10^5V/cm), the electrons produced by ionization that are very close to the nearest anode wire where the electric field is high, collide with the gas molecules and acquire enough energy to cause new ionisations. The secondary ionizations produce electron-ion pairs that cause other ionizations, resulting in a cascade of repeated ionizations and a large charge multiplication (electric charge avalanche effect) localized very close to the wire. The avalanche electrons reach the anode very quickly, inducing a fast negative signal on the specific wire, while the positive ions take much longer to reach the cathode due to their slow drift velocity and the larger distance they travel. The most significant contribution to the signal is due to this slow movement of the positive ions toward the cathode. Each anode wire is equipped with its electronic readout circuit, acting as an independent detector of a coordinate of the particle's position. The disadvantage of MWPC detectors is that their performance decreases as the particle rate increases; due to their slow drift velocity, the positive ions accumulate around the anode wires. Their accumulation distorts the electric field around the wires, thus reducing the induced signal. In addition, the distance between the wires (about 1 mm) limits their position resolution. Due to these limitations, new gas-filled detector technologies have been developed, such as the sTGC [27] and the NSW Micromegas.

The sTGCs [28] are multiwire gas chambers (2.8mm thick with a gas mixture of 55% CO_2 and 45% n-pentane) operating under high voltage (2.85kV). Their structure is shown in Figure 8. They consist of a grid of 50μm diameter gold-plated tungsten wires parallel to and 1.4mm apart from the two cathodes. The wires are spaced 1.8mm apart and are grouped in groups of 20. The outer surface of one of the two cathodes is grounded, while the inner surface has etched strips of copper perpendicular to the wires' plane. The spacing between the strips is 3.2mm, much smaller than that of TGCs (for this reason, these detectors are called small TGCs).

The other sTGC cathode is divided into large square readout pads on a 1.6mm thick PCB. The partitioning into surfaces was designed to reduce the number of strips used to determine the first-level triggering. For triggering, the sTGCs detectors must provide fast signals to determine the beams' collision point and reconstruct part of the muon trajectory with an angular resolution of less than one mrad. The trigger signal is determined nearly in real-time in two steps: In the first stage, the fast signals from the readout pads are used to identify muon trajectories originating from the collision point of the beams and to identify a region of interest (RoI) potentially containing high vertical momentum muon trajectories. In the second stage, the readout of the ROI strips is triggered to obtain an accurate measurement of the coordinate of the muon trajectory in the direction used to determine the muon momentum. The charge is induced in 3 to 5 strips and is processed to determine the centroid of the ROI strips' charge. Further processing of those centroids having an accuracy of 100μm together with the requirement that the trajectories must originate from the interaction point, results in reconstructing a portion of the trajectories to the required accuracy (1mrad). In addition, the signals from the readout wires determine the second coordinate of the trajectory (for which less accuracy is required) to improve the accuracy of the offline reconstruction of the trajectories. The charge from all the pads, strips, and wires is used for the offline reconstruction of the trajectory.

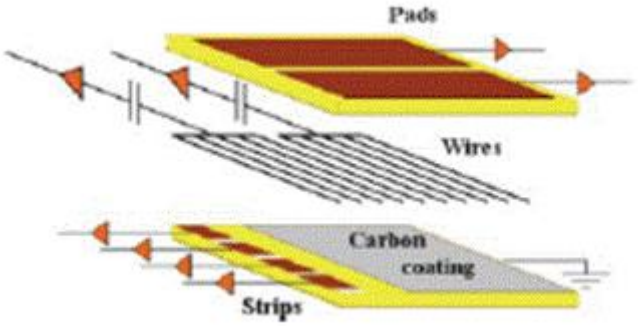


Figure 8: Graphical representation of the sTGC detector's structure[29].

2.2 The Resistive-Strip MicroMegas detectors

MicroMegas (Micro Mesh Gaseous Structure) detectors [30],[31] were proposed in the 1990s by G. Charpak and Y. Giomataris. They are gas-filled detectors belonging to the Micro-pattern gaseous detector technology (MPGD)[32], which was developed during the long research and development of detectors that can operate efficiently at high particle fluxes.

Their operating principle is based on the ionization of the gas filling as in the multi-wire analog chambers (MWPC), except that, thanks to microelectronics technology, the distance between their anode strips is of the order of a few hundred microns, and the distance between the anode-cathode electrodes is less than a millimeter, resulting in very good spatial and time resolution, and better operation in high particle flux conditions (due to the fast collection of positive charges, which reduces space charge effects).

The NSW detector system uses the innovative Resistive-strip Micromegas technology described in the following paragraphs. These detectors have the same operating principle as the Micromegas but extremely good operation in high particle flux conditions.

The structure of a MicroMegas (MM) detector is illustrated in Figure 9. Its novelty lies in replacing the wire level of MSGC detectors with a flat thin metallic micro-mesh (micromesh) [33] with tiny diameter holes and a distance between them in the order of a few tens of microns. The micromesh is supported by a system of insulating micromesh pillars of 300μm in diameter and 128μm high, printed in the plane of the readout anode. The entire detector assembly is located in an airtight environment filled with argon and small impurities of carbon dioxide.

The micromesh divides the detector into two regions:

(a) the 5mm thick conversion/drift region bounded by the cathode (drift electrode) plane and the micromesh plane.

(b) the amplification gap region defined by the micromesh and the plane of the anode (a PCB carrying 300 μm thick readout strips spaced 450μm apart, made of gold-coated copper).

The micromesh is used as an intermediate electrode for the electric field to be homogeneous in both detector areas. By applying an appropriate potential to the cathode and the micromesh, a relatively weak electric field is generated in the conversion/slip region (of the order of a few hundred V/cm), and a very strong electric field in the narrow amplification region (~40-50 kV/cm).

The need to fabricate low-cost MM detectors later led to the development of an innovative technique in which the entire region from the anode level to the micromesh is fabricated using Bulk Micromegas (PCB) technology [34].

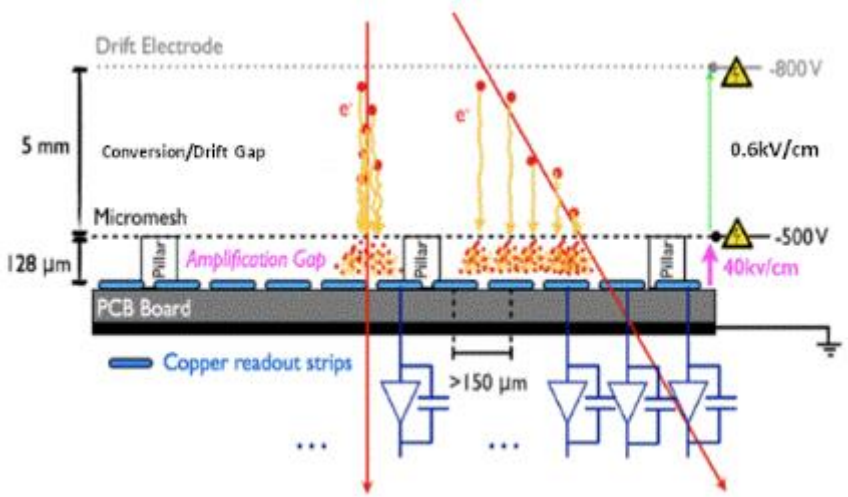


Figure 9: Cross-section of the MicroMegas detector, showing its functionality.

The detection mechanism in MM detectors is the ionization of the fill gas during the passage of a particle through the conversion/drift region. As in multi-wire chambers, due to the electric field of this region, the ions produced during ionization slide toward the cathode while the electrons slide toward the micromesh. The fact that the electric field in the enhancement region is 50-100 times greater than that of the conversion/slip region ensures that the micromesh is almost transparent (95%) to the electrons so that they enter the narrow amplification region (128μm) and very close to the readout strips the charge enhancement (charge avalanche mechanism) of the order of 10^4 is induced.

The anode microstrips collect the electron cloud produced by the avalanche mechanism while the positive ions drift in the opposite direction toward the micromesh. The creation of the avalanche occurs in less than 1ns, resulting in a very fast pulse induced in the readout strips, while the positive ions of the avalanche need a time of 100ns to reach the micromesh, which is very short compared to other detectors. This fast discharge of positive ions makes MM detectors suitable for very high particle fluxes.

The transverse growth of the induced signal is confined to a small area of the anode size bands of the amplification region; therefore, MM detectors of this type have a very good spatial resolution. Furthermore, the very good segmentation of the readout strips, together with the pretty good time resolution, enables the MMs to act as a complement to the triggering system of the NSW detector system based on sTGCs.

Despite their good performance, when exposed to high particle fluxes that cause a large ionization of the gas and the number of electrons produced during avalanche formation becomes larger than ~10^6, the MMs encounter the problem of sparking [35] between the micromesh and the readout strips. The sparks may create interruptions in the supply voltage resulting in a large dead time in operation and/or destruction of the detectors and readout electronics. This phenomenon is a major limiting factor for the efficient operation of the MM after the LHC upgrades. A protection scheme [36] was developed for the MM detectors used in NSW to overcome that problem. In particular, as shown in Figure 10, a thin (50-70μm) insulating layer of resistive strips with a resistance per unit length of a few MΩ/cm to a few tens of MΩ/cm has been introduced above the level of the microstrips so that the microstrips are not directly exposed to sparks. The resistive strips have precisely the same geometry as the readout microstrips, and their charge is induced to the readout microstrips connected to the electronic readout system.

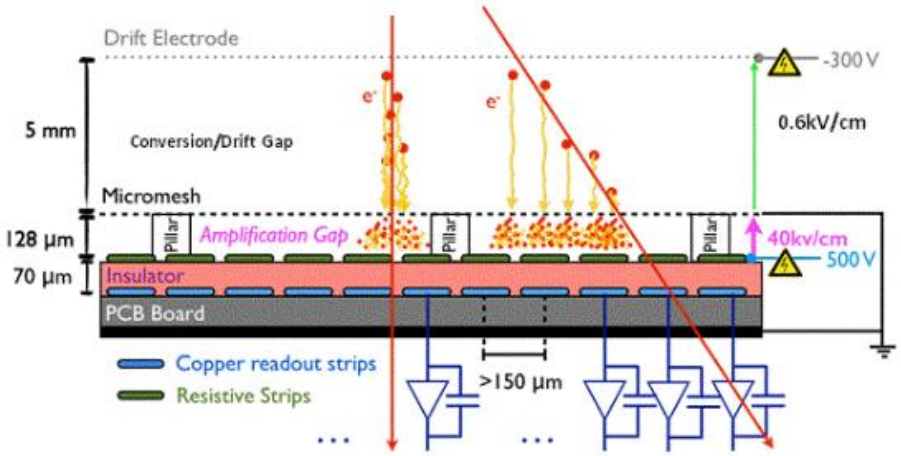


Figure 10: Cross-section of the MicroMegas detector, with the addition of resistive strips and the voltage adjustment in the micro mesh and readout strips.

Instead of a continuous resistive layer, the resistive microstrips were chosen mainly to avoid spreading the charge over several readout strips. Instead of applying a negative voltage to the micromesh, as in the typical MM structure, the micromesh is grounded, and a positive voltage is applied to the resistive strips (so that the current induced by the sparks is discharged very quickly to the ground through the micromesh while the potential of the micromesh does not change).

In addition, the MMs used in NSW differ in that the pulse readout is done by the readout strips and not by the micromesh, as in standard MMs.

In addition to the above modifications made to the NSW MMs, a different way has been adopted in their construction; the micromesh is no longer embedded in the PCB of the readout section of the detector (bulk micromegas) but has been integrated into an aluminum frame which is placed very precisely on the drift area. The micromesh is pressed against the readout frame's pillars, while the electrostatic force between the micromesh and the resistive strips ensures a good fit of the micromesh onto the pillars. That technique (mechanically floating mesh) (Figure 11) [37] has the advantage that the micromesh can be safely removed so that the amplification area is accessible (for example, in case of a cleaning need).

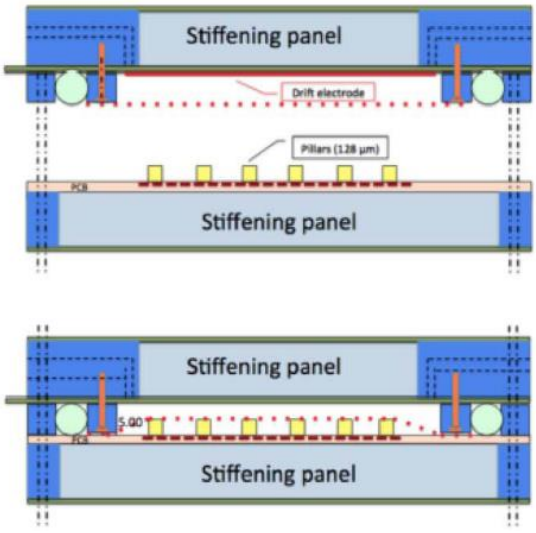


Figure 11: The assembly process of the MM detectors for the NSW.

2.3 The NSW muon spectrometer

Combining the two detection technologies, sTGC and MM, renders the NSW detection system a complete trigger and track detection system. The sTGC and MM detectors and their electronic systems were mounted on mechanical wheel-shaped support, tested, and then installed in the LHC tunnel at the ATLAS detector.

As shown in Figure 12, the NSW (about 10m in diameter) is divided into 16 trapezoidal-shaped radial sectors, eight small-sized sectors towards the Interaction Point (IP), and eight large-sized sectors in the opposite direction, which overlap to minimize dead regions and to have only areas of reduced detector performance.

The detectors of each sector are grouped in 4 wedges (2 for each type of detector) which are arranged along the axis of the collision of the beams, as shown in Figure 15 (sTGC-MM-MM-MM-sTGC). The detector layers of sTGC are divided into three segments, while those of MM are into two, each consisting of 4 detector layers (quadruplets).

Regarding the electronics system of the MM detectors, which is the subject of this thesis, each detector layer (wedge) consists of 8 PCBs with 1024 read channels each, so the electronic readout system of the MM detectors should handle about 2 million readout channels (while the readout channels of the sTGCs are about 300 thousand). In the readout system of the MM detectors, each PCB is connected to 2 readout cards (MMFE8), each of which has 8 ASICS (VMM) handling 64 channels. This system is described in detail in the next section.

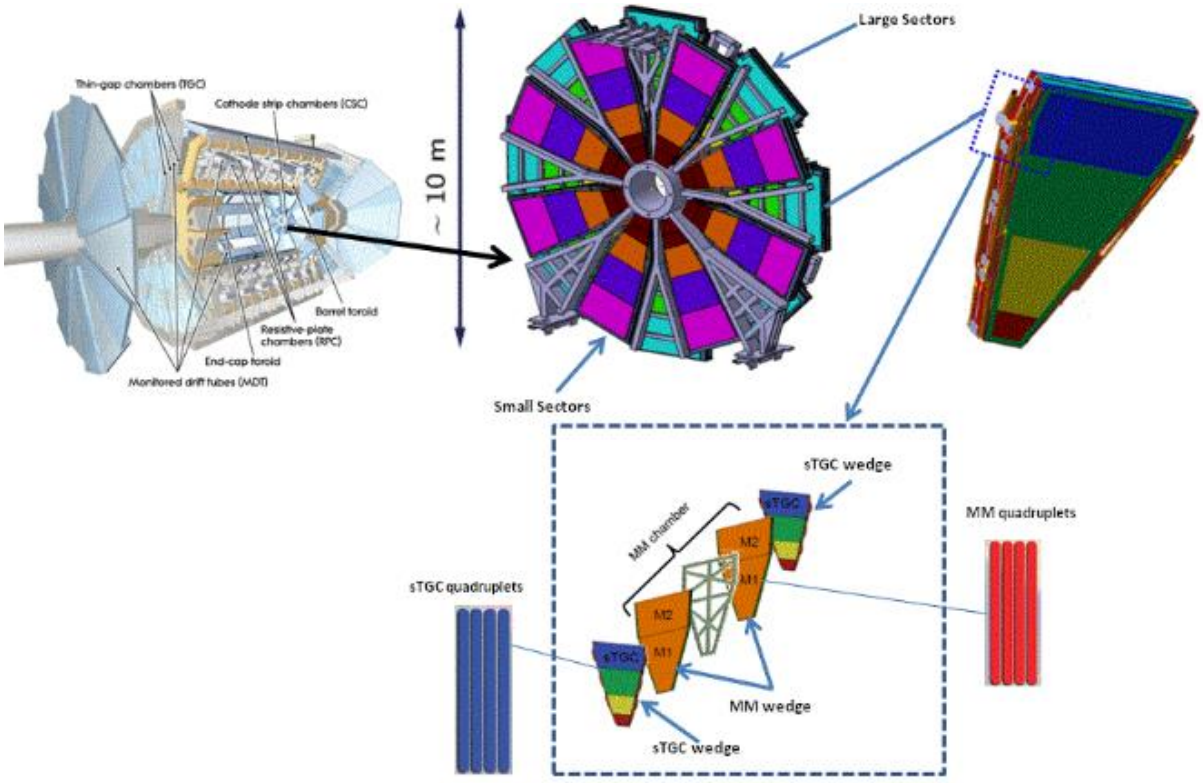


Figure 12: 3D models of the NSW and a large sector consisting of two MM and two sTGC wedges.

2.4 New Small Wheel electronics

In this section, the general structure and operation of the electronics system of the New Small Wheel (NSW) detection system are presented, which, as mentioned above, is expected to improve the muon triggering system in the front region of the Muon Spectrometer while

maintaining excellent detection capability of muon trajectories in a very high data flow and radiation environment.

The readout of the large number of NSW channels (2,097,152 channels of the MM detectors and 331,744 channels of the sTGC) in high data flux (21 kHz/cm^2 during operation after the second upgrade), radiation (radiation dose D=1700 Gy), and magnetic field (B=0. 4T) requires the construction of new electronic systems developed by the CERN and ATLAS research teams because the commercial-off-the-shelf (COTS) electronics are not sufficient. The above requirements for the electronics systems on the detectors must consider the small space available, the difficulty of access, and the low power consumption.

Regarding the trigger signals, after the first upgrade (2019-2022), a 100 kHz first-level triggering is required, while for the second upgrade (2024-2027), there are two schemes: a) 1MHz single-level triggering and b) two-level triggering with zero level triggering (Level-0 Accept) 1MHz and first level triggering (Level-1 Accept) 400 kHz.

Figure 13 shows a schematic representation of the NSW electronic system structure. The left side of the figure depicts the electronics on the detector in a high radiation and magnetic field region. These are the Front end boards-FEs, Level-1 Data Driver Card (L1DDC) [38], ART (Address in Real Time) Data Driver Card (ADDC)[39], Pad trigger, and Router, which consist of custom made radiation resistant Application Specific Integrated Circuits (ASICs). Communication between them will be done using mini Serial Attached Small Computer System Interface (SCSI) (miniSAS) cables.

On the right of Figure 13 are the off-detector electronics: the Front End LInkeXchange (FELIX) [40], Trigger processor, Sector logic, as well as services that run on commercially available Servers, such as Read Out Drivers (ROD), Detector Control System (DCS), event monitoring, configuration, trigger monitor and calibration. These are located in the ATLAS Underground Service Room (USA15), which is very close to the underground room where the ATLAS detector is located (outside of the magnetic field and radiation) and houses most of the detector electronics.

As shown in Figure 13, there are three different electronics chains, two for finding the trigger signal from the sTGC and MM detectors (trigger paths) and one chain for readout the data and controlling the electronics of the FEs (readout path) that is common to both types of detectors.

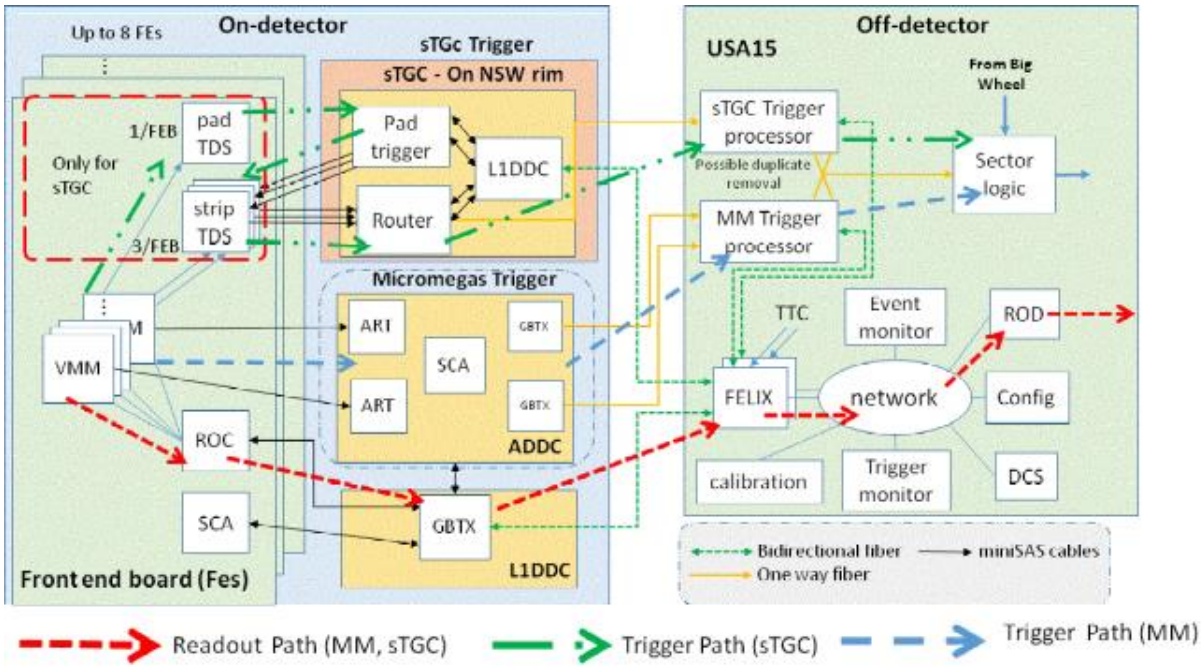


Figure 13: The Trigger and readout scheme of the NSW [39].

Due to the particular characteristics of the two different detector technologies MM and sTGCs, the FEs cards are different for sTGC and MM detectors.

The FEs cards of the MM detectors (MMFE8) consist of the following ASICs:

- A number of Venetios MicroMegas (VMM) ASICS [41] (up to 8 for MM and 6 for sTGC detectors). Each VMM accepts analog signals from 64 readout channels (corresponding to the strips of the detectors). Therefore, each MMFE8 can read 512 read channels of the MM detectors. Since there are approximately 2.1 million channels of MM detectors, 4096 MMFE8 cards were produced. The VMM ASIC performs two functions: a) sends to the two chains of trigger electronics (trigger paths) data used to determine the Level-1 Accept signal and b) sends data (after receiving a trigger signal) to the Level1 Data Driver Card L1DDC, which among other things is responsible for sending them to the electronics outside the detectors (readout path).
- A ROC ASIC (Readout Controller) [42]. The ROC is the first ASIC of the data readout electronics chain. It receives data packets from the eight VMMs of the MMFE8 (in the case of the MM detectors), i.e., from 512 different channels, and performs multiplexing, appropriate reconfiguration, and serialization to be routed over serial lines at 320 Mbs to the L1DDC.
- An SCA (Slow Control Adapter) ASIC. The SCA [43] is responsible for configuring and monitoring all cards and ASICs on the detectors.

The FEs cards of the sTGC detectors have, in addition to the VMMs (up to 6), the pad Trigger Data Serializer ASICs (pad-TDS) and strip Trigger Data Serializer (strip-TDS) ASICs [44] that are used to find the trigger signal from the sTGCs.

The two chains of trigger electronics operate independently of each other, and the information from each one is fused before being sent to the next trigger module. Thus, the trigger electronics chain from the sTGC detectors includes the pad/wire FEs and strip FEs, then the Trigger pad, Router, L1DDC, and finally, the Trigger processor module for the sTGCs

located outside the detectors. The electronics chain used to determine the trigger signal from the MM detectors includes the MMFE8 card sequence, the Address in Real Time Data Driver Card ADDC, and finally, the MM Trigger Processor.

In the MM detectors' trigger chain, the VMM ASICs of each MMFE8 send to the ADDC the address of the channel where the first detected charge deposit (hit) that is greater than its specific threshold (called address in real-time, ART). The ADDC is connected to 8 MMFE8 (64 VMMs). It has two Address in Real Time (ART) ASICs [45] that receive ART signals every 25ns from each VMM. The two ART ASICs multiplex the ART data and select in real-time to be routed to the GBTX ASICs [46] and then send them over optical fiber to the off-detector electronic trigger processor (MM Trigger Processor), which is a system of FPGA-based ATCA Mezzanine Cards performing the algorithms that determine the trigger signal. The ADDC also communicates with an L1DDC card which sends configuration data from the FELIX system [47] and provides timing signals. 1024 ADDC cards were constructed, tested, and installed in NSW (512 for MicroMegas and 512 for sTGC).

The two NSW MicroMegas and sTGC detector technologies, due to their significant differences in characteristics, geometry, and electronics, use different Trigger Processors with particular triggering algorithms each to reconstruct parts of the candidate tracks (trigger data) at each bunch crossing (BC) collision. These are sent to the Sector Logic [48] cards which match them with candidate track segments by the Big Wheel detection system to determine the final Level-1 Accept trigger signal. The Level-1 Accept signal is propagated via optical fiber from the FELIX system to the L1DDC card. The L1DDC (described in detail in the following subsection) is connected to eight MMFE8s and sends the Level-1 Accept signal so that the process of data readout from the ROC ASICs is triggered.

As mentioned above, the sequence of electronic cards used to read the data from the sTGC and MM detectors is common: the VMMs extract from the width of the recorded pulse in the stripes the information about the charge (hence the energy of the particle) and the information of the time (related to the beam crossing clock) of charge occurrence. They execute a selection algorithm, and upon arrival of a first-level trigger signal received from the ROC, they send the selected data to the ROC. The ROC stores the triggered events until a Level-1 Accept signal (L1) is received, selecting those to be routed to the L1DDC, then over fiber at 4.8Gbps to the FELIX system, and finally to the Read Out Devices (RODs).

The L1DDCs are radiation and magnetic field tolerant boards handling the exchange of data between the Front-End boards (FE) and the off-detector FELIX network. These boards were designed by the National Technical University of Athens (NTUA) team in cooperation with Brookhaven National Laboratory (BNL) in New York. The primary purpose of the board is to handle three distinctive paths of data: the Timing Trigger & Control (TTC), the Data Acquisition (DAQ), and the Slow Control (SC), as shown in Figure 14. The key component, which defines the functionality of the L1DDC, is the GBTx ASIC, which can aggregate up to forty Electrical Links (E-Links) into a single fiber. The rest of the components comprising the board is the Slow Control Adapter (SCA), the FEAST 2.1 DC-DC converter, the Versatile Twin Transmitter (VTTX), and the Versatile Transceiver (VTRX) optical modules. Three different types of L1DDC boards have been designed to meet the requirements of the two detector technologies: The MicroMegas (MM-L1DDC), the sTGC-L1DDC, and the Rim-L1DDC. The following sub-sections will discuss the three types of L1DDCs, their prototypes, and their basic components.

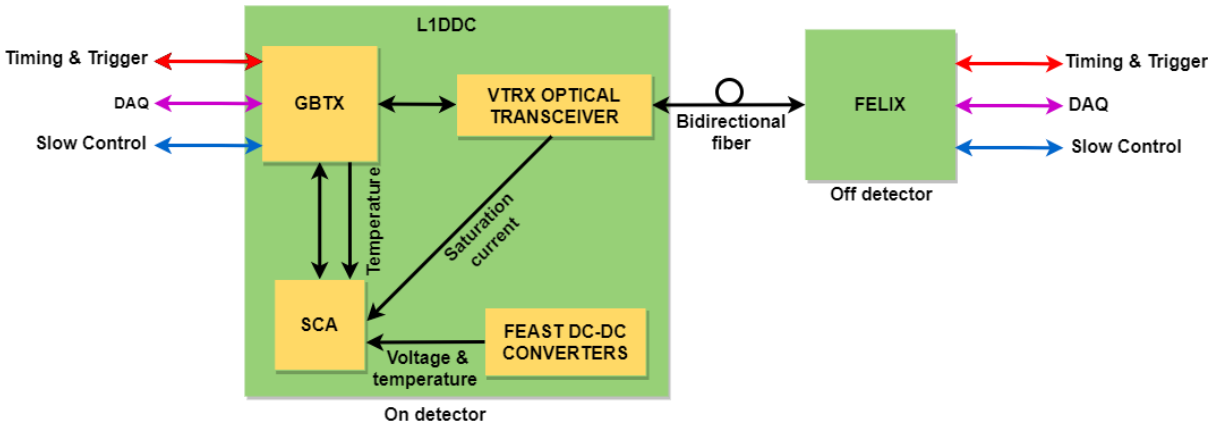


Figure 14: A simplified block diagram of the L1DDC, showing the three data paths.

The MM-L1DDC front-end side is connected with eight MM FEs and one ART Data Driver Card (ADDC), the sTGC-L1DDC with three sTGC FEs, while the RIM-L1DDC interfaces with the on-detector trigger electronics of the sTGC detectors (one PAD trigger and eight router boards) via duplex Electrical serial Links (E-Links). For the interconnection with the on-detector electronics through the E-links, the L1DDC has 36 miniSAS connectors. The back-end side of all three L1DDC types communicates with FELIX via bi-directional optical fibers (at a rate of 4.8 Gb/s).

3.1 The GBTX ASIC

As mentioned before, the basic component of the L1DDC is the GBTX ASIC. The GBT project, and subsequently the GBTX, is part of the radiation-hard optical link project (a project aimed to develop a radiation-hard, bi-directional optical link between the on-detector and the off-detector electronics for use in the LHC upgrade programs). The GBTX's functionality can be viewed as a multiplexer/demultiplexer (Figure 15).

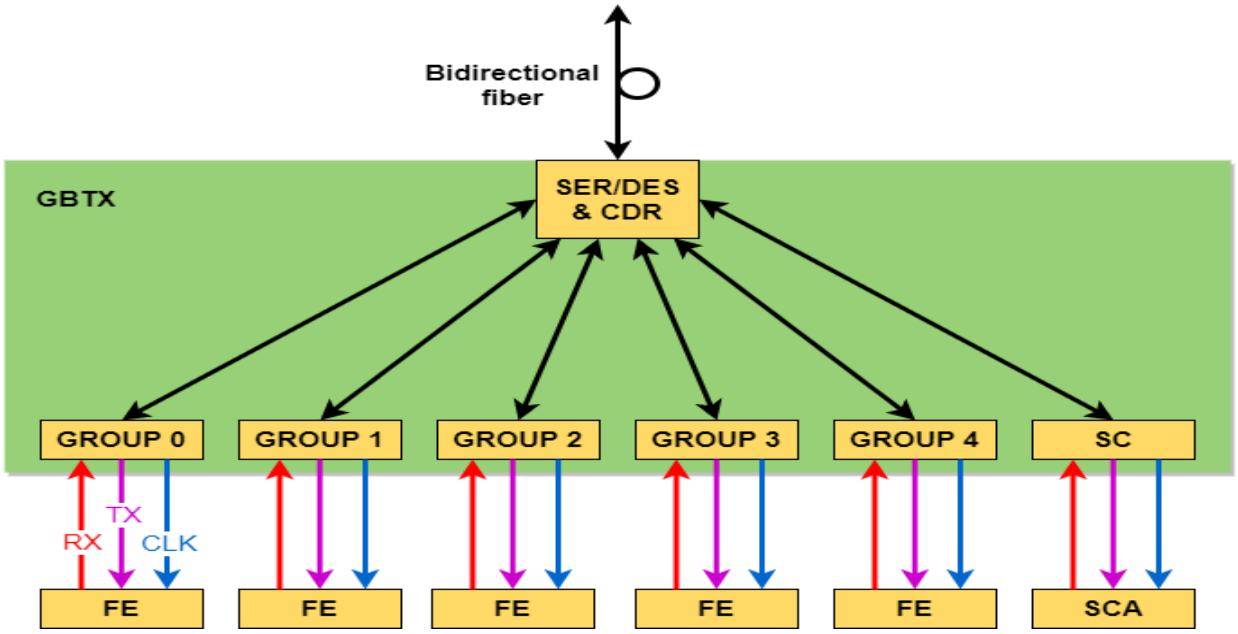


Figure 15: A simplified block diagram of the GBTx, showing the optical data deserialization into E-Links and vice versa.

The connection between the L1DDC and the front-end boards is accomplished through serial E-Links, where each consists typically of three differential pairs:

- The differential Clock line (dCLK+/dCLK-): Clock driven by the GBTX to the FE board.
- The differential Downlink data output (dOut+/dOut-): Data driven from the GBTX to the FE board.
- The differential Uplink data input (dIn+/dIn-): Data driven from the FE board to the GBTX.

Up to 40 E-Links can be multiplexed to form a single frame over multimode fiber and vice versa. The E-links are divided into five independent groups where each group can support: eight E-Links at a rate of 80 Mb/s, four E-Links at 160 Mb/s, and two E-Links at 320 Mb/s. Additionally, the GBTX has one extra E-Link, the External Control (EC), with a fixed data rate of 80 Mb/s targeted for communication with the SCA ASIC. The interfacing with FELIX, GBTX, and subsequently the L1DDC utilizes the 120-bit GBT frame format, which is transmitted or received during a single LHC bunch-crossing interval of 25ns resulting in a rate of 4.8 Gb/s. The GBT frame pictured below (Figure 16) consists of the following:

- The Header: indicates whether the frame contains actual data or a synchronization frame. It has a length of four bits with two valid combinations.
- The Internal Control (IC): a link that operates at 80 Mb/s for the configuration of the GBTX's registers. The protocol for this link resembles the HDLC protocol, but a Longitudinal Redundancy Check is used instead of the Cyclic Redundancy Check for the frame check sequence.
- The External Control: As mentioned before, its primary purpose is to communicate with the SCA. However, it can be used as a regular E-Link for different purposes.
- The Data field: consists of 80 bits for the forty E-Links. Each one takes up two bits when the rate is 80 Mb/s, four bits when the rate is 160 Mb/s, and eight bits at 320 Mb/s.

- The Forward Error Correction (FEC) field: The 32 bits of the FEC code are assembled by two interleaved Reed-Solomon encoded words with four-bit symbols. Practically a sequence of 16 consecutive errors can be corrected.

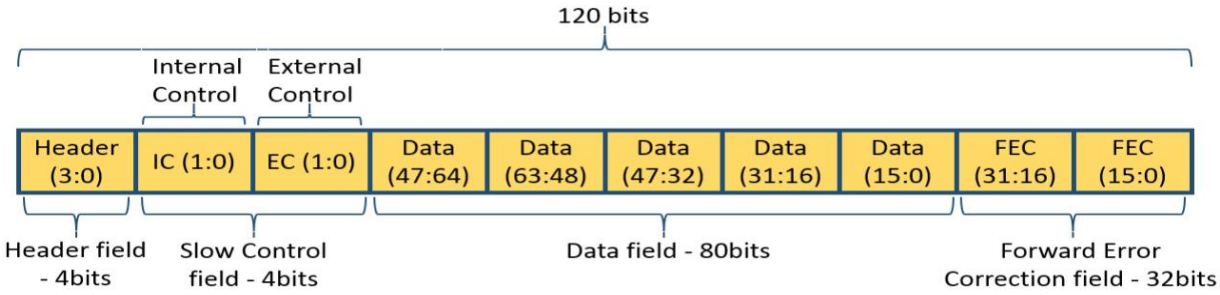


Figure 16 *The GBT frame format*

The GBTX's architecture, as seen from the Fes' side, comprises the phase aligners where the phase of the data received from the FEs is adjusted, so sampling is performed at the center of the data eye.

Following the phase aligners, the data are driven to the Scrambler logic to obtain DC balance, encoded and interleaved with the FEC code, and finally serialized to form the GBT frame to be sent to the optical module. On the other hand, the received GBT frame is used for Clock Data Recovery, then is deserialized, deinterleaved, decoded where the possible errors can be corrected, descrambled, and finally driven to the E-Links serializers. The recovered clock from the GBT frames is also forwarded to the FEs through the E-Link clock line. The E-Link clock's frequency is set to 40 MHz for all the E-Links of the L1DDC, although GBTx can also deliver 80, 160, and 320 MHz clocks. For the operation of the control logic of the GBTX, an on-chip 40 MHz crystal is used. The configuration of the GBTX is setup by 366 user programmable registers, many of which use Triple Modular Redundancy circuitry to achieve robustness against Single Event Upsets (SEU). Each register has a particular one-time programmable E-fuse. Thus, the most suitable configuration can be written to the E-fuse bank, which will be copied to the registers during the power-on sequence. A dedicated GBTX programmer, through the I^2C port of the GBTX, can access the E-fuses along with the registers. After the initialization of the GBTX (in case it is configured in transceiver mode), the registers can also be accessed by the IC channel through the optical link.

3.2 The GBT-SCA ASIC

The GBT-SCA ASIC is part of the GBT chipset and is designed to extend GBTX's functionality. The purpose of the SCA (Figure 17) is to distribute control and monitoring signals to various front-end ASICs, such as the ROC, TDS, and VMM ASICs, along with FPGAs. To meet these requirements, SCA implements a set of different interfaces. These include 16 independent I^2C masters, one Serial Peripheral Interface (SPI) master, one Joint Test Action Group (JTAG), 31 analog inputs multiplexed to a 12-bit Analogue to Digital Converter (ADC), and 32 General Purpose Input-Output (GPIO) signal pins.

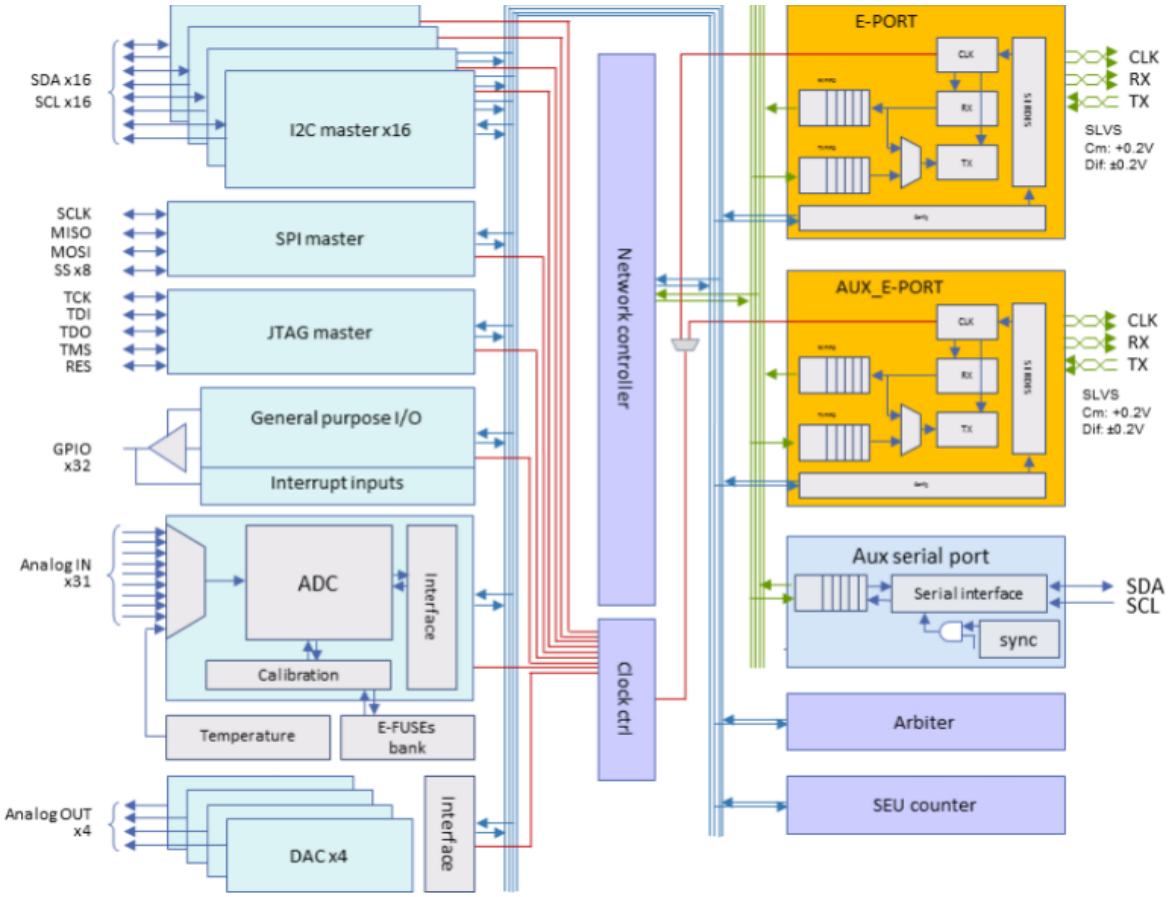


Figure 17: GBT-SCA block diagram, showing the different communication interfaces, the GPIO, the ADC, and DAC interfaces.

The communication between the SCA and the GBTX is established by the dedicated EC E-Link of the GBTX. This dedicated E-Link runs at 40 MHz Double Data Rate (DDR) mode, providing an effective data rate of 80 Mb/s. It is also possible to connect the SCA to any other E-Link as long as its data rate is configured to 80 Mb/s. This feature allows multiple SCAs (up to 41) to be accessed by a single GBTX. Since GBTX is transparent to user data, a remote system in the control room forms a two-layer protocol to communicate with the SCA. The first layer is the E-Link transport protocol based on the HDLC standard (ISO/IEC 13239:2002), where the HDLC frame's payload is formed by the second layer, named SCA channel command protocol (Figure 18).

Furthermore, radiation-tolerant design techniques have been employed to protect the operation of the SCA against radiation-induced SEU, making it compatible with the phase-2 run.

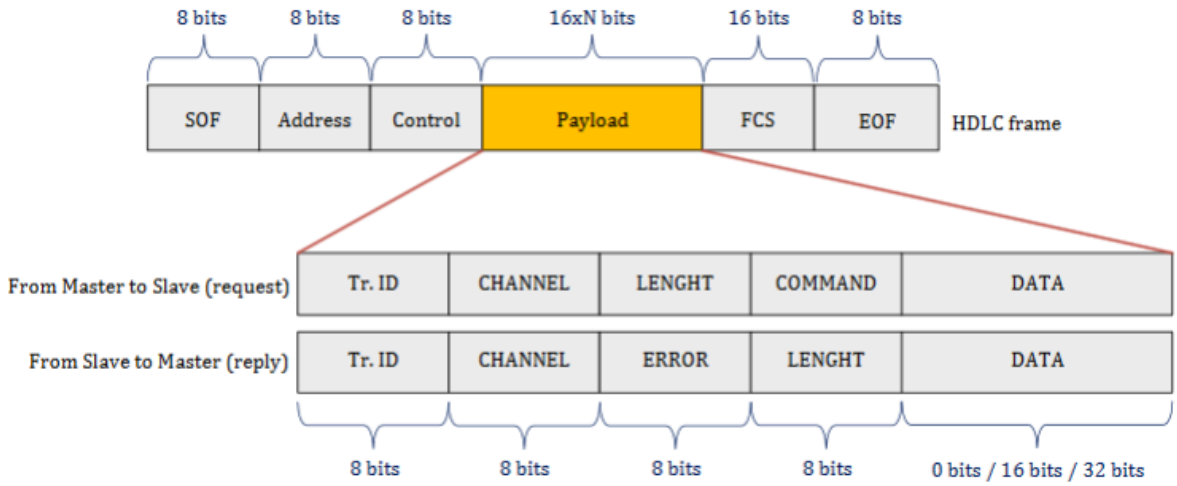


Figure 18: The SCA communication protocol over the HDLC protocol.

3.3 The VTRX & VTTX optical modules

The VTRX and the VTTX optical module (Figure 19) were developed under the joint ATLAS-CMS Versatile Link project. That project aims to produce a radiation and magnetic field-tolerant optical receiver/transmitter with low mass, volume, and power consumption.

The VTRX consists of two ASICs; the GigaBit Transimpedance Amplifier (GBTIA) and the GigaBit Laser Driver (GBLD). The GBTIA is a 5Gb/s highly sensitive optical receiver with low power consumption (120 mW) and 2.5V supply voltage. The irradiation testing of the ASIC proved that no performance degradation occurred with a radiation dose of 200Mrad. The GBLD laser driver can achieve a 5Gb/s rate with a power consumption of 325mW. Similarly to the GBTIA, GBLD can withstand a radiation dose of 200 Mrad.

Figure 19: Left: A commercial SFP+ optical transceiver. Middle: The VTRX transceiver. Right: the VTTX dual transmitter.

3.4 The FEAST2.1

The FEAST2.1 is a synchronous step-down converter developed at CERN for various High Energy Physics experiments. It can continuously operate up to more than 200 Mrad total ionizing dose and an integrated particle fluence of 5 × 1014 n/cm^2 (1MeV-equivalent). In addition, it is designed for operation in strong magnetic fields of more than 40000 Gauss, and the switching frequency is selectable in the range of 1 to 3 MHz. The frequency setting for the L1DDCs is 1.5 MHz. The input voltage range is 5V to 12V, and the maximum continuous current is up to 4A. FEAST features protection mechanisms for over-current, over-temperature, and input under-voltage. An analog output (PTAT) for internal temperature monitoring is also available.

3.5 The MM-L1DDC

The Micromegas detectors comprise approximately 2.1 million readout channels. The readout of these channels requires 4096 MMFE8 boards; each one of the boards consists of eight VMMs (32768 in total) and ROC ASICs. Each VMM is capable of readout 64 MM channels. The trigger scheme of the MM consists of the MMFE8, the ADDC boards (512 in total), and the MM Trigger Processor. In total, 512 MM-L1DDCs were used for the MM detectors, each connected with eight MMFE8 boards and one ADDC board. The purpose of the MM-L1DDC is:

- To communicate with the ROC and the SCA of the MMFE8 boards. The downlink (from the control room to the detector) path of the communication provides configuration data for the ROC, the SCA and the VMMs, along with the 40 MHz LHC Bunch Crossing Clock (BC Clock) and trigger data. On the other hand, the Uplink path (from the detector to the control room) contains the data from the VMMs collected by the ROC and monitoring data, such as the output voltages of MMFE8's FEASTs, temperature measurement of the ASICs, and the readout of the ASICs configuration.

Table 1: The TTC frame format.

MSB = 7	6	5	4	3	2	1	0
L1A	Soft Reset	Test Pulse	ECR	BCR+OCR	L0A	SCA Reset	EC0R

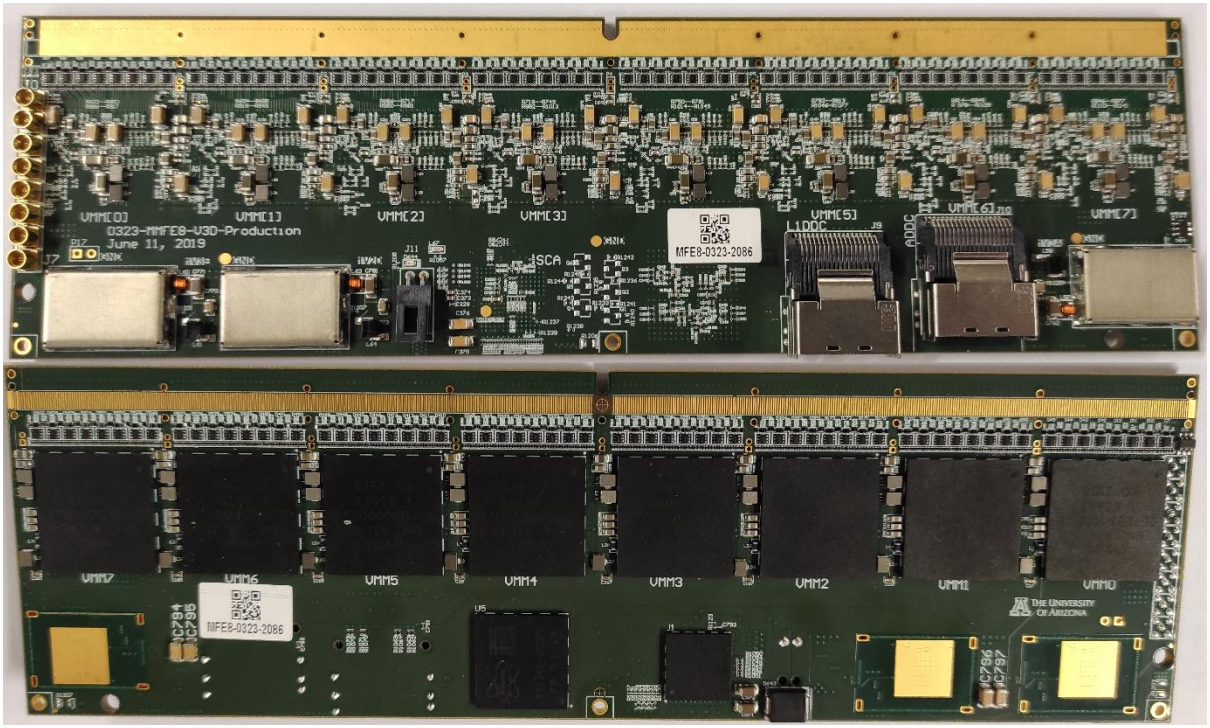


Figure 20: The top and bottom view of the MMFE8 board.

- To communicate with the two GBTXs and the SCA of the ADDC board. The downlink path distributes configuration data for the GBTXs and the SCA, two reference clocks for the GBTXs, two Bunch Crossing Reset (BCR) signals, and a reference clock for the BCR. The uplink path provides the read back of the configuration data and, as in the MMFE8 case, voltage and temperature measurements.

Initially, the specification for the Level-1 trigger rate was set to 200kHz; later, it was increased to 400kHz; finally, the requirement was set to slightly below 1MHz. This increase in the Level-1 rate resulted in higher data rates for the DAQ scheme; thus, L1DDC had to accommodate a larger number of GBTXs. The evolution of the MM-L1DDC from the first prototype to the final production design is described in the following subsections.

3.5.1 Prototype 1

The first multifunctional L1DDC prototype board (Figure 21) was designed and fabricated in 2014 by the NTUA group. This initial design was common for both Micromegas and sTGCs detectors. Prototype 1 hosted one GBTX (version 1) and a Xilinx Artix-7 Field Programmable Gate Array (FPGA) chip as a redundant solution in case of GBTX failure. Several multiplexers and voltage translators were used to switch between the two chips. Moreover, the two alternative paths were used to compare the data between them. In addition, during the first tests of the board, the FPGA acted as a Front-end and FELIX emulator, where data from the FPGA were sent to GBTX, received back, and checked for errors.

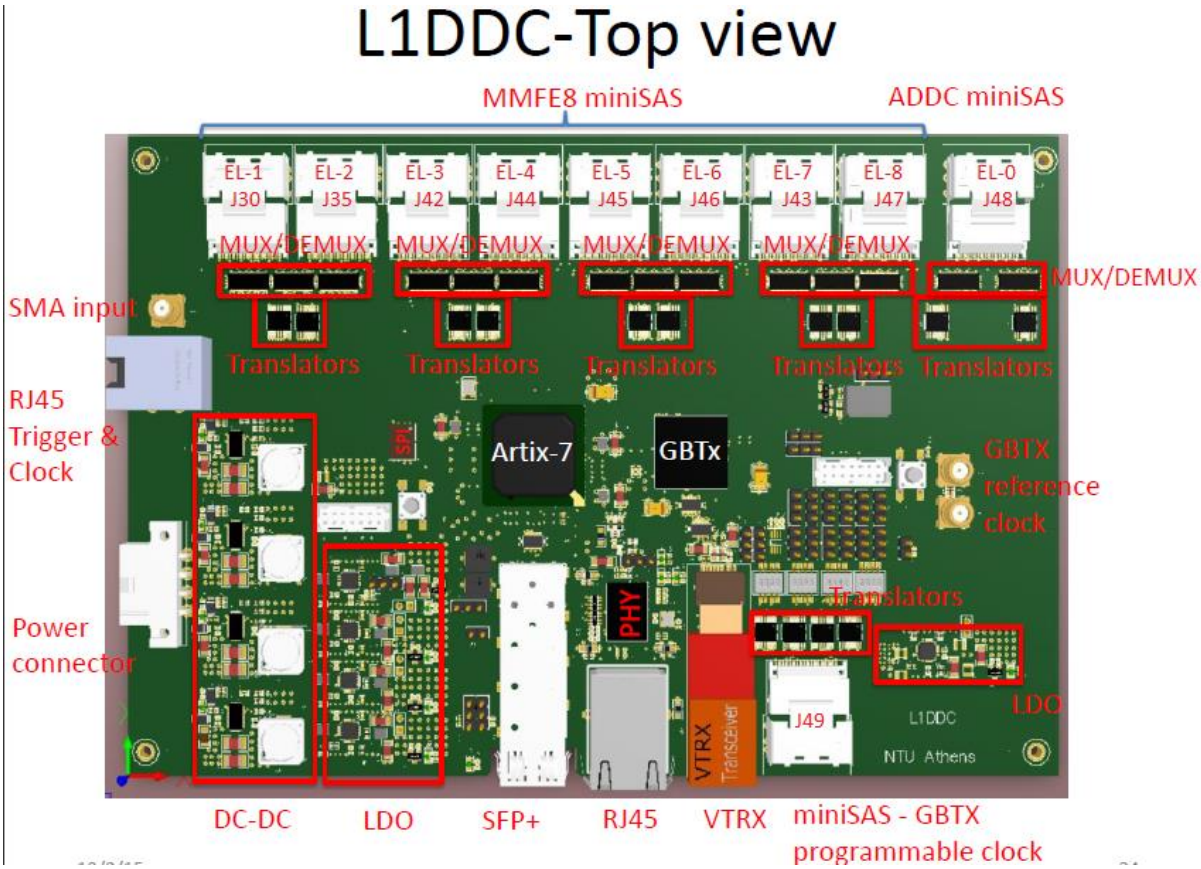


Figure 21: 3D model of the L1DDC prototype 1.

The main components comprising prototype 1 were:

- One GBTX version 1.
- One Xilinx Artix-7 XC7A200T-3FBG484 FPGA.
- One VTRX and one Small Form-Factor Pluggable (SFP+) optical transceiver. The FPGA and the GBTX could utilize both of those transceivers via multiplexers.
- 10 Mini Serial Attached Small Computer System Interface (MiniSAS) 36-pin connectors. Eight of them were dedicated to the MMFE8 boards, one to the ADDC, and one to measurements of GBTX's programmable clocks's outputs.
- One RJ45 connector and an Ethernet physical interface chip (capable of 1Gb/s data rate Ethernet connection with the FPGA).
- Four Linear Technology LT8612 DC-DC converters with an input range of 3.4V up to 42V
- Five ADP1755 linear Low DropOut (LDO) regulators from Analog Devices to step down the outputs of the DC-DC converters.
- 17 multiplexers/demultiplexers.
- 10 Voltage level translators.
- Several DIP switches and jumpers to switch between different signal sources and set logical values for testing purposes

3.5.2 MM-L1DDC prototype 2

Given the new specification for a Level-1 trigger rate of 1 MHz, prototype 2 (Figure 22) had significant differences from prototype 1. Additionally, by the time this prototype was designed, version 2 of GBTX was released. Three GBTXs were needed to meet this requirement. One of the GBTXs was configured in transceiver mode, and the other two as transmitters. Thus, bi-directional communication is achieved with only one GBTX, and a VTRX is used for that purpose, while the two transmitter GBTXs share the VTTX optical transmitter. Since bi-directional communication with that two GBTXs is impossible, one SCA ASIC driven by the transceiver GBTX is configured through the I^2C port. Moreover, unnecessary components, such as the FPGA, the RJ45 connector, and the multiplexers, were removed, and the commercial DC-DC converters and LDOs were replaced with the radiation-tolerant FEAST DC-DC converter. Finally, the board size was reduced to 200mm×64mm to fit the position holes of the detector.

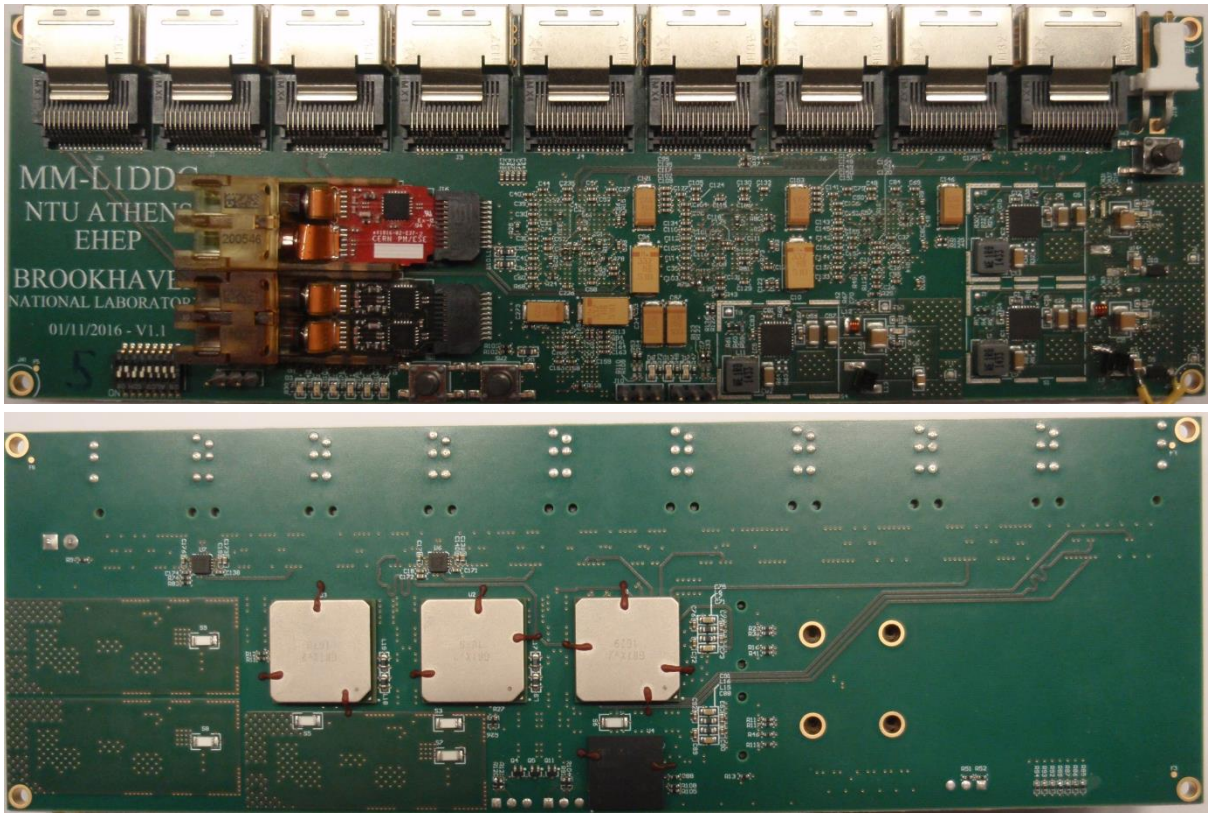


Figure 22: Top and bottom view of L1DDC prototype 2

The components comprising prototype 2 are as follows:

- Three GBTXs Version 2.
- One VTRX and one VTTX optical module.
- Three FEAST DC-DC converters. Two of them provide 1.5V for the GBTXs, and the third powers the VTRX and VTTX at 2.5V.
- Two Microchip Technology SY54011RMG, 1:2 fanout chips were used. The necessity of these chips resides in the lack of enough E-Links at 320Mb/s for the TTC data. An alternative solution would be to use one more GBTX, but it would have resulted in an even more complex design, increased power consumption, and cost.

- Nine MiniSAS connectors, eight for the MMFE8 boards, and one for the ADDC.

3.5.3 MM-L1DDC prototype 3, pre-production and production design

Prototype 3 of the MM-L1DDC (Figure 23) had the same dimensions as prototype 2, but several additions and modifications were made. After testing prototype two, it was revealed that with the suitable configuration of the GBTXs, the power consumption was significantly lower than expected. For that reason, the second 1.5V FEAST DC-DC converter was removed. Additionally, the layout of the FEAST was changed to become the same as the layout recommended by the FEAST design team for uniformity with the rest of NSW electronics. The rest of the modifications included:

- The usage of two more fanout chips for the clock (to meet the number of transmitting clocks necessary for the MM scheme).
- The relocation of ADDC's MiniSAS (to allow a smaller-length twinax cable to be used). Also, one more Bunch Crossing Reset (BCR) signal was added to the connector as the ADDC design team requested it.
- The removal of the DIP switches (subsequently, all the configuration pins were hardwired).
- The replacement of ferrite beads (used to decouple and filter the VTRx, VTTx, SCA, and GBTx ASICS) with ceramic inductors.
- The replacement of temperature sensors (used to measure the temperature of GBTXs) with the DC95F502WN made by Amphenol Advanced Sensors.
- The correction of design errors found in the previous prototype.

After prototype 3 testing, the reviewers accepted the design, and the pre-production phase was launched. The modification for this phase includes replacing tantalum capacitors with ceramic, replacing the power connector with Molex nanofit, the standard for on-detector electronics, and replacing the ceramic inductors with shielded inductors. Eventually, 50 pre-production boards were fabricated and tested extensively. Following the pre-production phase, the production phase was initiated. The production design of the MM-L1DDC is almost identical to the pre-production one, except for a PCB cut-out close to the VTRX/VTTX optical modules to fit a bracket for the cooling of the optical modules.

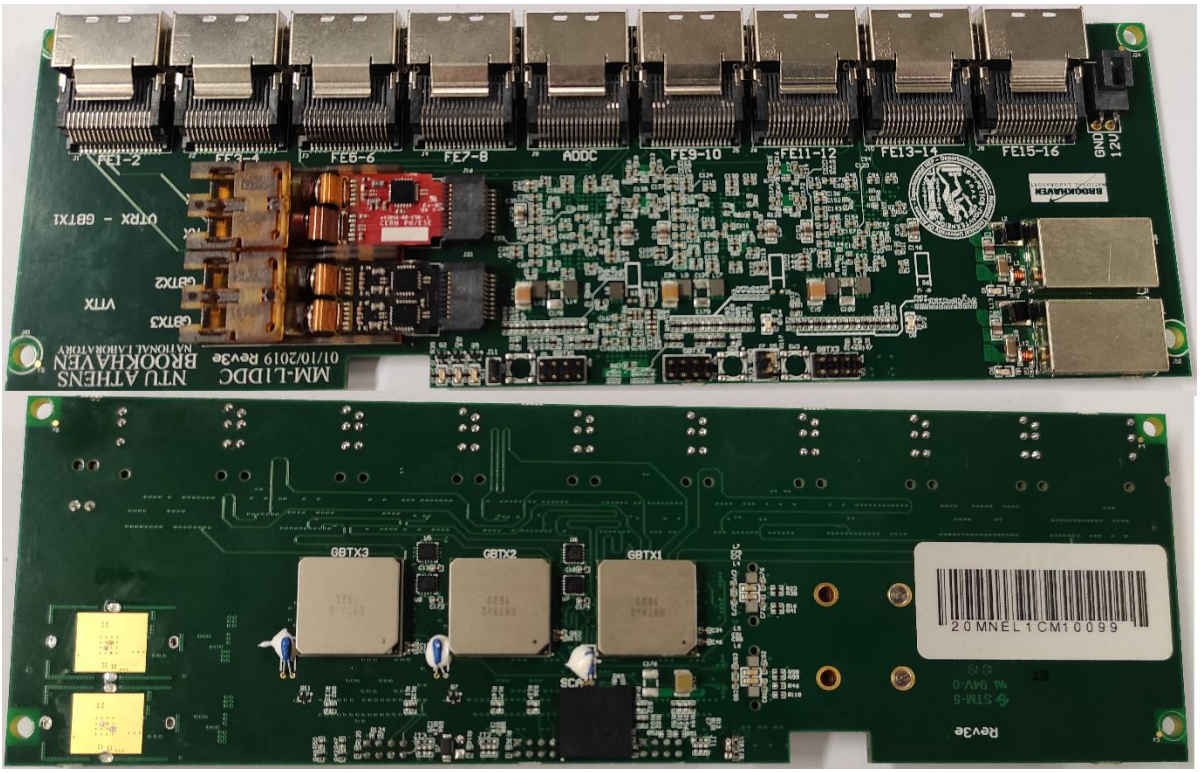


Figure 23: Top and bottom view of the final L1DDC design.

3.6 The sTGC-L1DDC

The sTGC detectors comprise 400 thousand readout channels. This detector technology uses two types of front-end boards: the Strip Front-End Board (sFEB) and the Pad Front-End board (pFEB). The sFEB consists of eight VMMs, four Trigger Data Serializers (TDS) ASICs, one ROC, and one SCA, whereas pFEB features three VMMs, one TDS, one ROC, and one SCA ASIC. In total, 768 sFEBs and 768 pFEB were installed on the sTGC sectors for the NSW project. As shown in Figure 24, the trigger scheme for the sTGCs is more complex than the one of the Micromegas, including the two types of FEBs, the PAD trigger, the Router boards, the sTGC-L1DCC, the sTGC Trigger Processor, and the Rim-L1DCC.

The purpose of the sTGC-L1DDC is similar to MM-L1DDC:

- The sTGC-L1DDC is responsible for the communication with the ROC and the SCA of the pFEBs and the sFEBs. The downlink (from the control room to the detector) path of the communication provides configuration data for the ROC, the SCA, the TDS, and the VMMs, along with the 40 MHz LHC Bunch Crossing Clock (BC Clock) and trigger data. On the other hand, the Uplink path (from the detector to the control room) contains the data from the VMMs collected by the ROC and monitoring data, such as the output voltages of FEB's FEASTs, temperature measurement of the ASICs, and the readout of the ASICs configuration.
- Furthermore, the sTGC-L1DDC provides 2.5V output for the powering of the sTGC trigger path repeaters.

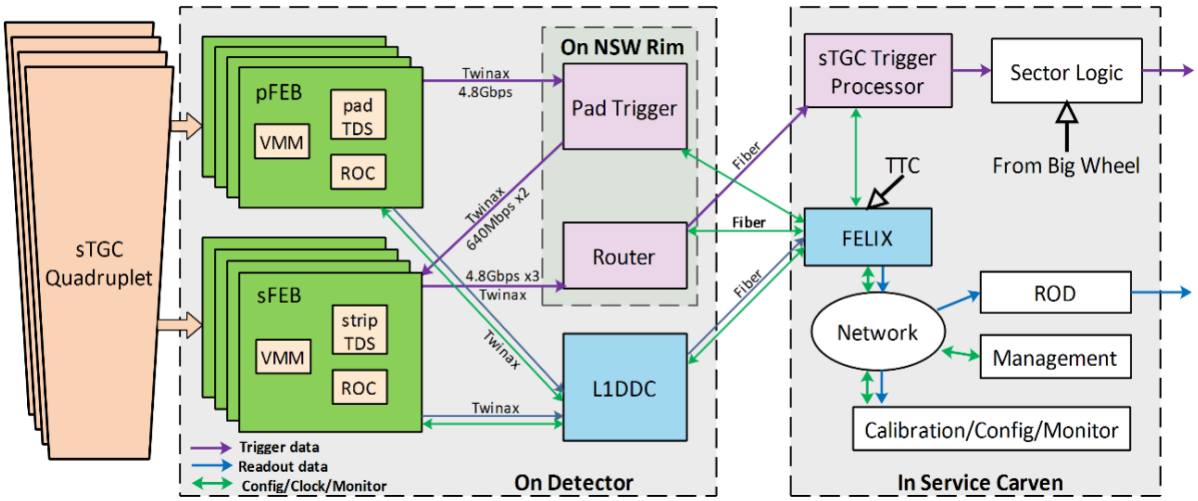


Figure 24: The sTGC readout and trigger data path.

3.6.1 sTGC-L1DDC prototype 2

As mentioned earlier, prototype 1 was a shared design for both detector technologies. Later, different boards were designed for each detector to meet the 1 MHz readout rate requirement. Prototype 2 (Figure 25) was the first L1DDC designed to fulfill the specifications of the sTGC detectors exclusively. Since the sTGC detectors have much fewer readout channels than the MM, fewer Front-End boards are used, and subsequently, the sTGC-L1DCC has only two GBTXs. Each one of the GBTXs is configured in transceiver mode and has its own VTRX module. Thus, both can achieve bi-directional communication with FELIX, and the optical link can independently configure each one. The boards' dimensions were set to 140mm×60mm.

The main components comprising prototype 2 are:

- Two GBTXs (version 2)
- Two VTRX optical transceivers.
- Two FEAST DC-DC converters. One of them provides the 1.5V for the GBTXs, and the second powers the VTRXs at 2.5V.
- Four MiniSAS connectors (dedicated to the Front-Ends).
- Two sets of DIP switches (for the configuration pins of the GBTXs).

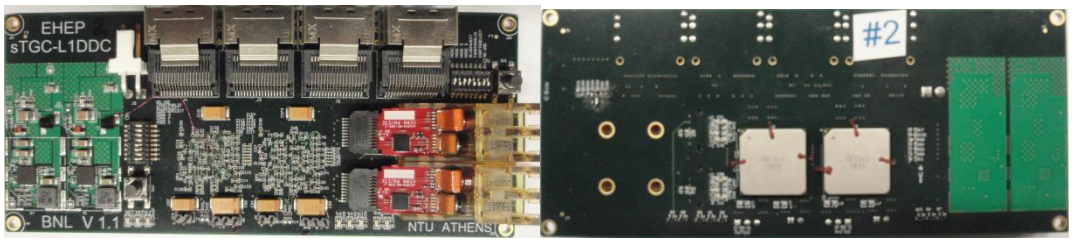


Figure 25: Top and bottom view of the sTGC-L1DDC prototype 2.

3.6.2 sTGC-L1DDC prototype 3

During the design of the Low Voltage (LV) box, which contains the low voltage distribution boards for the sTGC electronics, it was found that the dimensions of the box conflict with the LC fiber connector of the L1DDC. Thus the board was redesigned with significantly less length, 125 mm×60 mm, compared to the 140 mm×60 mm of prototype 2. The most notable modifications of prototype 3 are:

- The relocation of the VTRXs to the center of the board
- The redesign and reduction of the size of the FEAST layout (to reduce space and to become more uniform with the layout recommended by the FEAST design team).
- The replacement of ferrite beads (used for decoupling and filtering) with ceramic inductors.
- The removal of the DIP switches (subsequently, all the configuration pins were hardwired).
- The Rx polarity of the VTRX on prototype two was found to be swapped and corrected.

3.6.3 sTGC- L1DDC prototype 4, pre-production and production design

For prototype 4 (Figure 26), the sTGC team requested some additional features. These include the addition of an SCA ASIC, temperature sensors for the GBTXs, and one extra power connector. The SCA on the sTGC-L1DDC is used mainly for monitoring the FEAST output voltages and the temperature of the GBTXs. The I^2C port is a redundant path for the GBTXs' configuration. In that sense, each GBTX can be configured by its own IC field of the GBT-frame, and it can configure its other through SCA's I^2C. Moreover, the extra power connector of prototype 4 was used to provide 2.5V to serial and LVDS repeaters of the sTGC scheme. In order to gain some space on the board to host the mentioned additional features, FEAST's layout was again redesigned, with smaller form factor passive components and new custom-made shields.

The design of prototype 4, with minor changes, was accepted by the reviewers to proceed to the pre-production phase. For this phase, 50 boards were fabricated and tested extensively. There was no need for further design modification, and subsequently, the pre-production design entered the mass production phase, where 522 boards were fabricated and tested, as described in the next chapter, to fulfill the needs of the sTGC detectors.

Figure 26: Top and bottom view of the final sTGC-L1DDC design

3.7 The Rim-L1DDC

The Rim-L1DDC interconnects the on-detector sTGC trigger electronics with FELIX. Since only one Rim -L1DDC will be used for each NSW sector (32 boards in total), in case of

failure, the trigger path of the whole sector will be rendered inoperable. For this reason, the RIM-L1DDC was designed to be redundant and separated into two independent and identical parts (Figure 27), the primary part and the auxiliary.

The objective of Rim -L1DDC is to:

- Provide a low jitter 160 MHz clock for the transceivers of the FPGAs on the PAD trigger and router boards.
- Distribute 80Mb/s configuration and monitoring data.
- Provide 160Mb/s TTC data to the router boards and 320 Mb/s TTC data to the PAD trigger.
- Distribute a synchronous 40 MHz clock of the LHC proton-proton BC clock to the PAD trigger and router boards.
- Receive 80Mb/s monitoring data from the SCAs.
- Receive 160Mb/s and 320Mb/s Level-1 data for the router boards and the PAD trigger, respectively.

3.7.1 Rim-L1DDC prototype 1

For the communication with the eight router boards and the PAD trigger board, one GBTX is almost enough to handle the data traffic. Prototype 1 utilizes the eight programmable clock outputs of the GBTX to distribute the 160 MHz reference clocks. Since nine reference clocks are needed, a 1:2 fanout chip was used. Furthermore, a VTRX is used for the optical link with the FELIX. Finally, FEAST DC-DC converters were used to power the GBTx, the VTRX, and the fanout chip. As Rim-L1DDC is designed with redundancy, all the above hardware was doubled.

3.7.2 Rim-L1DDC prototype 2 and production design

Prototype 2 of the Rim-L1DDC (Figure 28) features several differences from its predecessor. The layout was redesigned so that the primary and auxiliary circuits were independent. Furthermore, a mechanism for powering on and off the routers and PAD trigger was requested by the Rim electronics designers; therefore, two SCAs were added to the design (one for the primary and one for the auxiliary part of the board). The General Purpose Input Output (GPIO) port of the SCA was used to drive the enable signals of the FEASTs on the routers and PAD trigger boards. Moreover, the SCA was also used to monitor the temperature of the GBTX, the voltages of the FEASTs and each one of the primary and auxiliary SCAs are capable to communicate and configure both the primary and auxiliary GBTX. After testing prototype 1 with the PAD trigger board, it was discovered that the 160MHz clock generated by the GBTX was marginally good for the transceivers of the Xilinx 7-series family. A second VTRX was utilized to receive a stable 160 MHz clock transmitted by the clock distribution board to overcome this issue. For redundancy purposes, each part of prototype 2 has five different reference clock sources that can be selected through multiplexers driven by SCA's GPIO port. For the primary side of the board (equally for auxiliary), the source of the reference clock can be driven by: the primary dedicated VTRX, the auxiliary dedicated VTRX, two E-

link clocks of the primary GBTX, and one E-Link clock from the auxiliary GBTX.

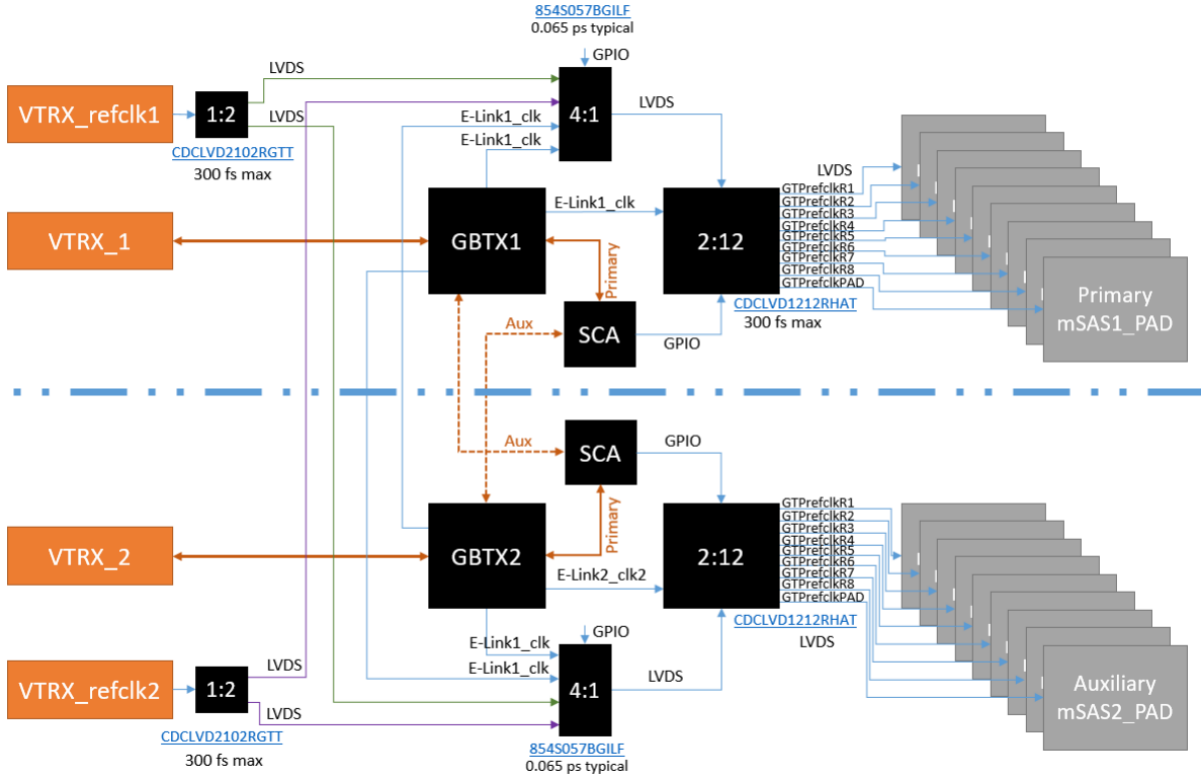


Figure 27: Block diagram of the Rim-L1DDC, showing the primary and redundant side of the board.

The prototype 2 design was accepted for the pre-production phase, where two boards were fabricated. For the production phase, the placement of a copper bar for the cooling of the VTRXs was requested. For that reason, a slight design modification was made to accommodate four holes on the PCBs to lock place the cooling bar. Finally, 40 Rim-L1DDCs were fabricated for the whole NSW project.

The main components comprising each side of the production design of the Rim-L1DDC are listed below:

- One GBTX (version 2)
- One SCA
- Two VTRXs (one for the communication with FELIX and the second for the dedicated clocks).
- Two FEAST DC-DC converters (they power the GBTX, the SCA, and the rest of the chips).
- One CDCLVD2102 1:2 fanout buffer by Texas Instruments (to fanout the dedicated clock).
- One 854S057B LVDS 4:1 clock multiplexer by IDT (to switch between the different reference clock sources).
- One CDCLVD1212 2:12 fanout buffer by Texas Instruments (to fanout the selected reference clock source into nine clocks).

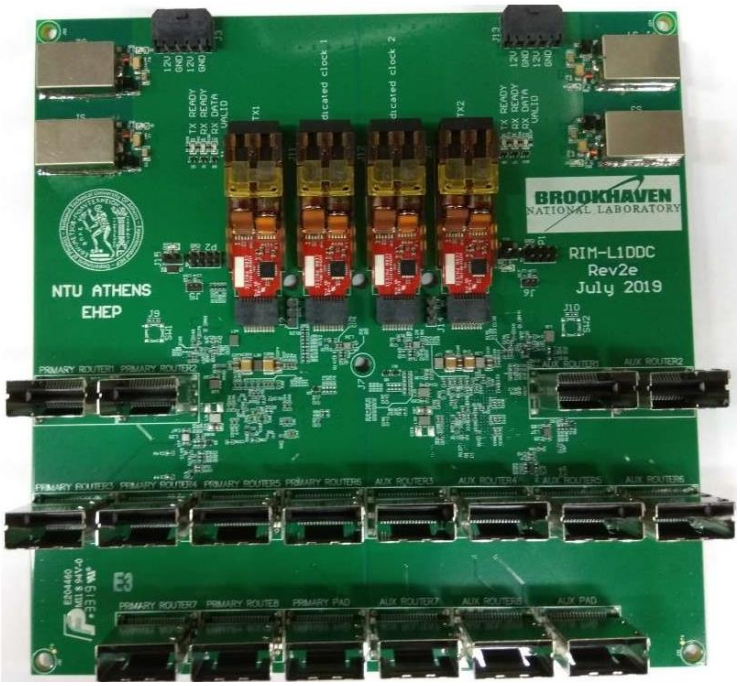


Figure 28: Top view of the final Rim-L1DDC design.

During the design and the development of the L1DDCs, extensive tests were required to verify the functionality of the boards. For the tests, dedicated FPGA firmware and hardware were developed. A testing setup was assembled using several commercial and custom-made boards, accompanied by the FPGA firmware and software developed for this purpose. As the various L1DDC prototypes were designed, the testing hardware and firmware evolved to meet the increasing requirements.

4.1 Hardware

As shown in Figure 29 and in Figure 30, the testing setup consists of the following hardware modules; the L1DDC to be tested, one Xilinx VC709 evaluation board, one Texas Instruments CDCE62005 clock generator/jitter cleaner, one custom-made FPGA Mezzanine Card (FMC) with nine mini-SAS connectors and a PC. The VC709 evaluation board is a commercial product featuring a Virtex-7 FPGA, one FMC connector, and four SFP+ optical transceivers. Three SPFs establish an optical bi-directional link between the L1DDC and the VC709, while the fourth serves as an Ethernet link between the VC709 and the PC. The clock generator is configured to generate and provide to the VC709 a 120MHz clock as a reference for the Multi-Gigabit Transceivers (MGT). The FMC board enables the interconnection of the L1DDC's miniSAS connectors with the VC709's FPGA.

In addition, an I^2C–USB dongle is used to fuse the configuration registers of the GBTx and to read/write its registers for debugging purposes.

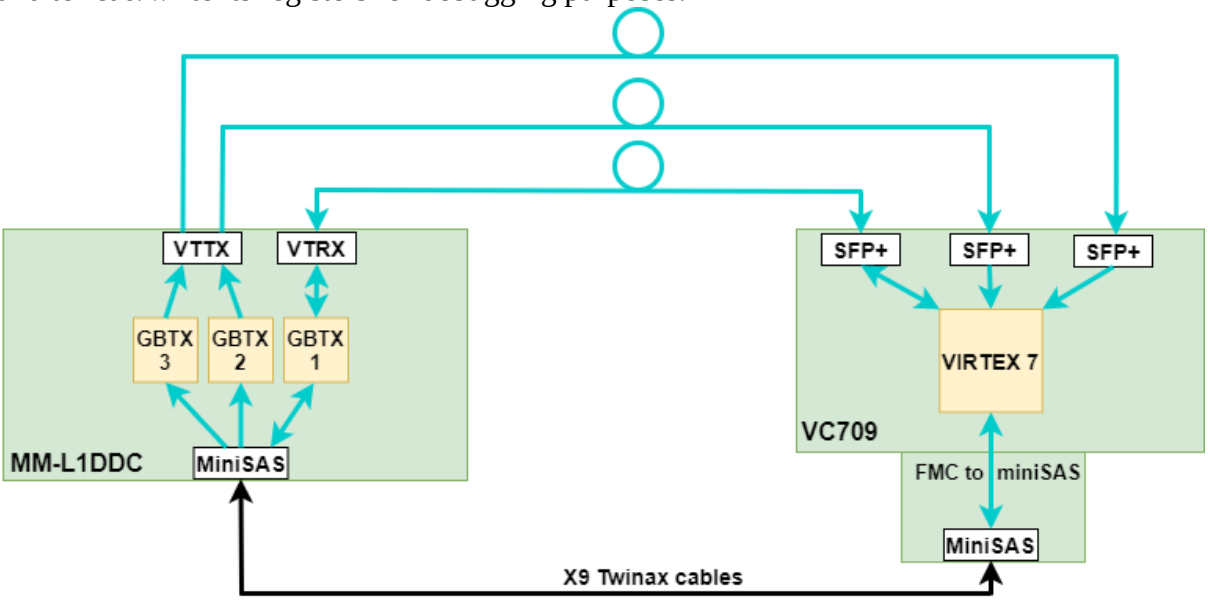


Figure 29: MM-L1DDC test setup block diagram.

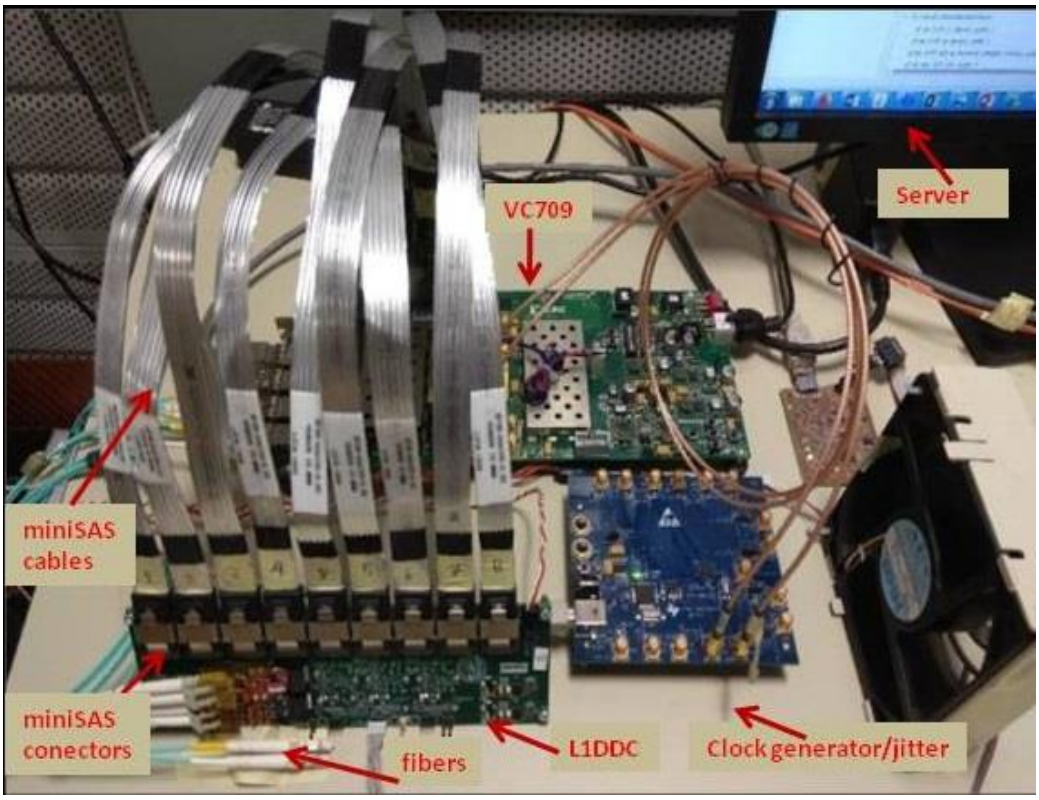


Figure 30: L1DDC testing setup.

4.2 Firmware

Dedicated firmware was developed for each type of L1DDC (MM, sTGC, and RIM). A simplified block diagram of the test setup is shown in Figure 31**,** representing the logic of all three types. The firmware development started in the early stages of the L1DDC prototyping and evolved as new prototypes were designed and new specifications of the testing procedure were set. Initially, the firmware was implemented as a stand-alone FPGA tester, consisting of the GBT-FPGA core, which emulates the core function of the GBTx, and the Electrical Link Interface (E-Link Interface), which mimics the data exchange with the FE boards. Later in the development, the GBT-Slow Control (GBT-SC) and the 1Gb/s UDP Ethernet cores were added. The former handles the External Control communication with the SCA and the Internal Control communication with the GBTx, and the latter, the communication between the firmware and the L1DDC test software. The following subsections describe the functionality of all these cores in more detail.

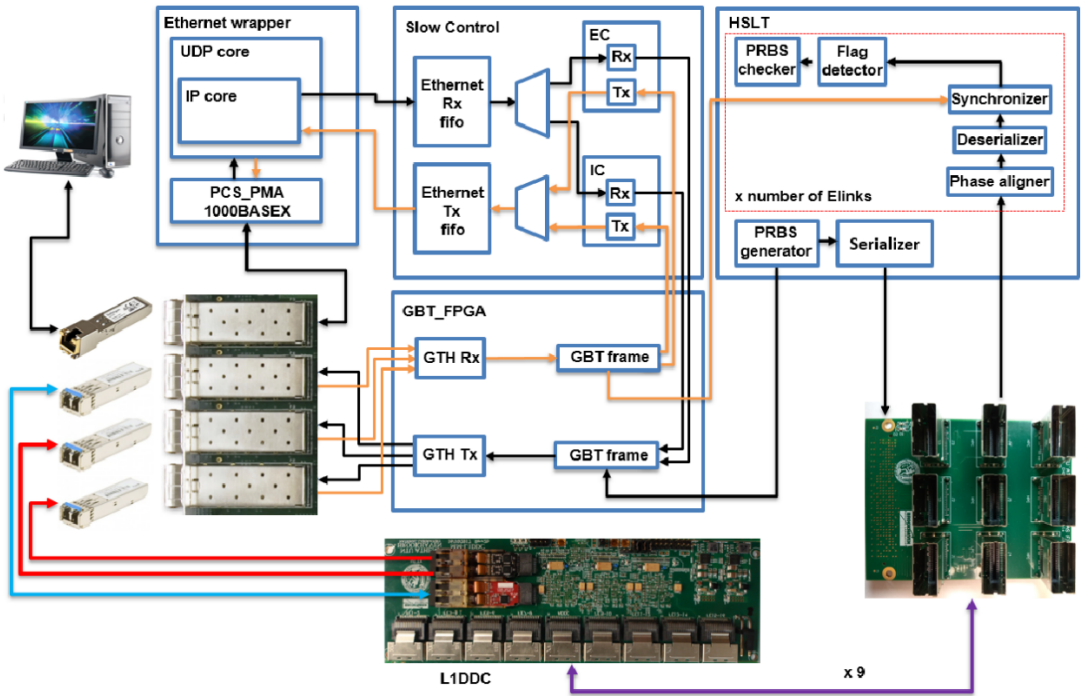


Figure 31: Testing firmware block diagram.

4.2.1 The GBT-FPGA core

Initially, the GBT-FPGA was developed by the GBT Project team [49] to emulate the GBTx serial link and test the first GBTx prototypes. As the GBTx users' requirements inflated, the GBT-FPGA evolved into a complete library targeting the FPGAs of the main vendors: Altera and Xilinx. Therefore, the different components of the GBT-FPGA Core are integrated into a single module called "GBT Bank." Each GBT Link comprises a GBT Tx, a GBT Rx logic, and a Multi-Gigabit Transceiver (MGT), as shown in Figure 32.

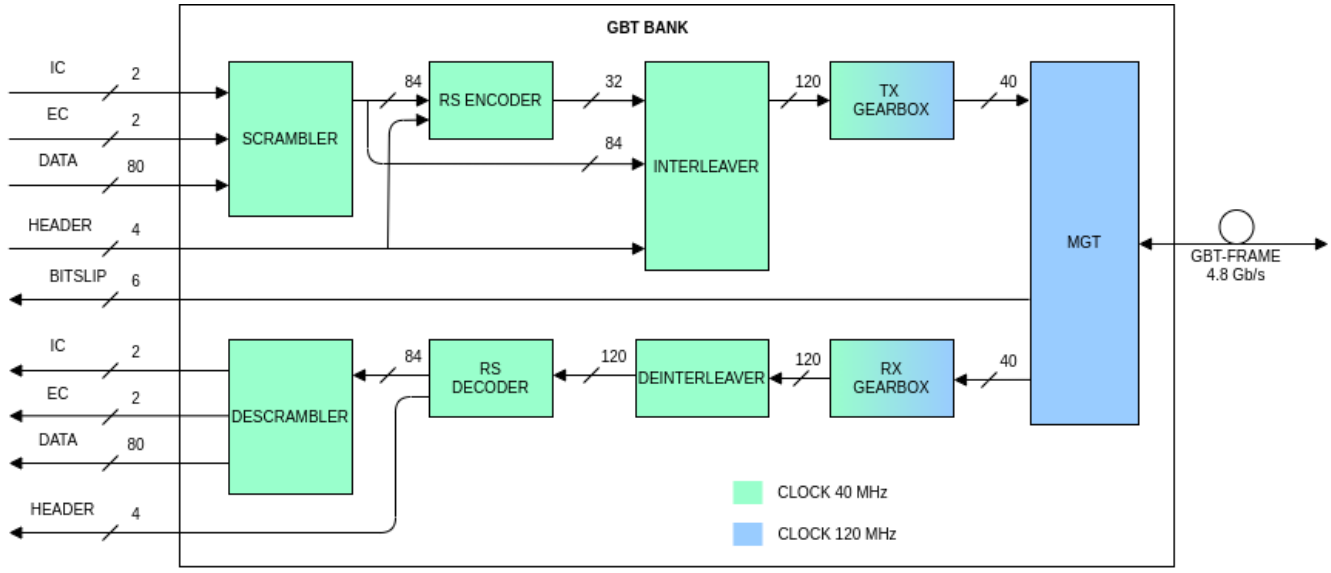


Figure 32: GBT-FPGA GBT-Bank logic.

The interfacing with the GBT-Bank is mainly done by four different data buses (the rest of the control signals are omitted for simplicity), the IC, the EC, the header, and the data bus.

As mentioned in chapter 3.1, the IC data form an 80Mb/s link for configuring and monitoring the GBTx implementing the IC protocol. The EC channel, also at 80 Mb/s, is used for communicating with the SCA ASIC implementing the SCA-HDLC protocol. The data bus is arranged by the user into five 16-bit groups. Three data rates are possible for every group: 1) two links of 8-bits resulting in a data rate of 320Mb/s (40MHz × 8 bits), 2) four four-bit links at 160Mb/s, and 3) eight two-bit links at 80Mb/s. Additionally, the Header bus has two possible values: "0110" and "0101". The former indicates that the GBT-Frame is a synchronization frame and does not contain valid data, while the latter indicates that the GBT-Frame contains valid data. For the L1DDC testing, the bitslip signal from MGT, which shows whether the 4.8Gb/s link with the GBTx is stable or not, is used to set the type of header. As long as the link with the GBTx is unstable, no valid data are transmitted. One GBT-Bank is used for every L1DDC GBTx, where the data rate of each group is defined to match the corresponding group of the GBTx under test in the L1DCC.

4.2.2 The E-Link Interface

The main component for the performance validation of the L1DDC is the E-Link Interface. The UniWA group designed this component to provide a reliable, self-synchronizing mechanism for sending and receiving data and error detection. The development of the E-Link Interface began from the early prototype phase of the L1DDC and evolved to meet the requirements of the final L1DDC types. Additionally, it is worth mentioning that the E-Link interface was used for other projects, such as the testing of the sTGC repeaters and the testing of the Mini-SAS cables of the MM sectors.

The purpose of the E-Link Interface is to emulate the data streams from the FEs to the L1DDC and vice versa while checking for errors. Consequently, the E-Link interface consists of two main components: the E-Link Transmitter and the E-Link Receiver. These components comprise different subcomponents, which will be discussed in the following subsections.

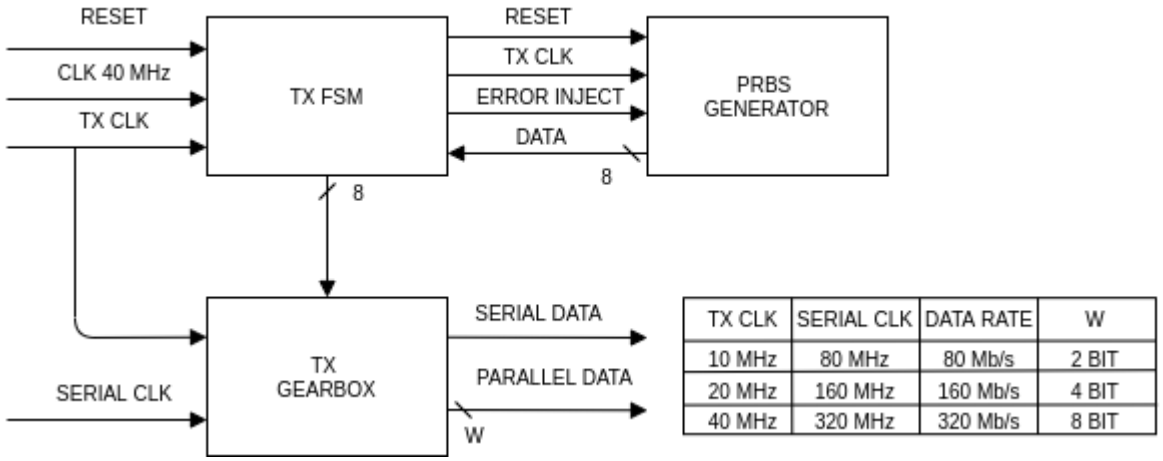
4.2.2.1 The E-Link Transmitter

The E-Link Transmitter is responsible for data generation and transmission. Three instances of the transmitter were designed, each one for the three data rates needed for the L1DDC testing, e.i. 80Mb/s, 160Mb/s and 320 Mb/s. The E-Link Transmitter consists of three subcomponents: the data generator, the TX Finite State Machine (FSM), and the Tx gearbox, as shown in Figure 33. The data generator uses the Xilinx Pseudo Random Binary Sequence (PRBS) [50] generator to generate the eight-bit characters to be sent. The PRBS generator is configured to use the $x^7 + x^6 + 1$ polynomial (PRBS7). This polynomial is not a telecommunication standard, but it is used because it is very similar to the 8B10B encoding used by the FEs. It is worth mentioning that the early L1DDC prototypes were tested with a custom generator and not with the PRBS. The PRBS generator is controlled by the TX FSM, which provides the clock and reset signals. The TX FSM eight-bit output consists of an idle byte, the start of the packet, 113 bytes with the PRBS data, and the end of the packet. These extra bytes were added to the stream to deliver the PRBS data in a frame format, as shown in Table 2.

Table 2: The E-Link Interface frame format.

Start of packet	PRBS7 data	End of packet	Idle
0x7E	0xXX	0x7E	0xFF

The purpose of this format is to make the E-Link Interface Receiver self-synchronized. Finally, the eight-bit data from the TX FSM are sent to the TX Gearbox. The gearbox converts the data a) in a serial stream of the requested data rate, which is sent directly to the L1DDC to emulate the FE data stream, or b) to parallel data (of 2-bits at 8Mb/s, 4-bits at 160Mb/s, and 8-bits at320Mb/s), which are sent to the GBT-FPGA and through the optical link to the L1DDC, to emulate the FELIX data stream.



TX CLK	SERIAL CLK	DATA RATE	W
10 MHz	80 MHz	80 Mb/s	2 BIT
20 MHz	160 MHz	160 Mb/s	4 BIT
40 MHz	320 MHz	320 Mb/s	8 BIT

Figure 33: E-Link Transmitter block diagram.

4.2.2.2 The E-Link Receiver

The E-Link Receiver is responsible for the reception of the data transmitted by the E-Link Transmitter and passed through the L1DDC. One Receiver is instantiated for every L1DDC E-Link, emulating the receiver part of the FEs and FELIX. The architecture of the Receiver is more complicated compared with the transmitter one due to the synchronization processes. As shown in Figure 34, the Receiver consists of four sub-components: the Synchronizer, the Phase Aligner, the Flag Detector, and the Frame Decoder-Error Detector. Three types of the E-Link receiver were designed for every possible data rate, i.e., 80Mb/s, 160Mb/s, and 320Mb/s. Also, each implementation has a selection bit to accept serial (directly from the L1DDC or parallel data (from GBT-FPGA).

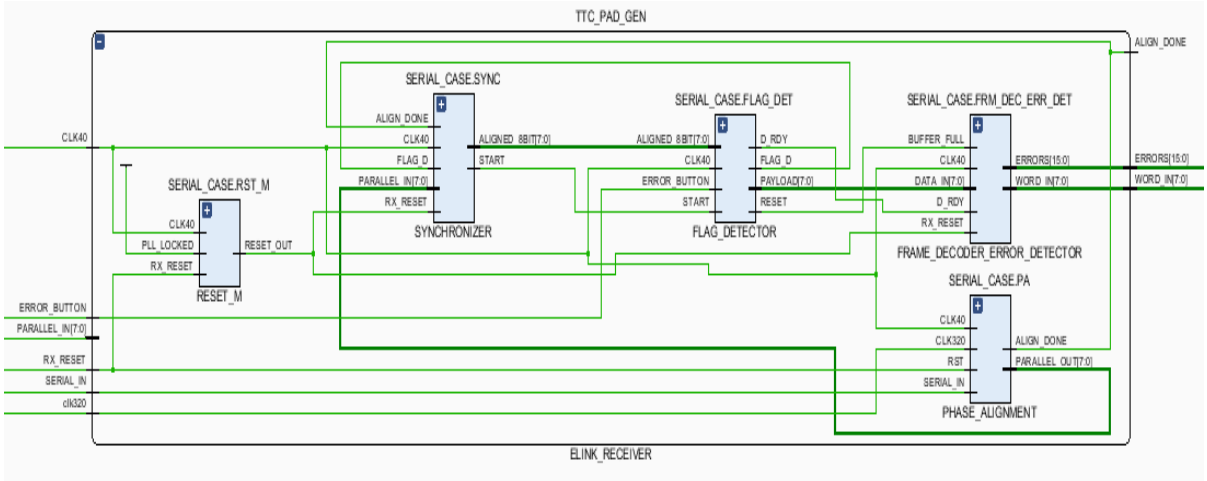


Figure 34: The E-Link Receiver block diagram.

The primary clock frequency of the L1DDC testing firmware is 40MHz, the exact frequency used by the electronics in the actual experiment. For this purpose, all the necessary clocks (such as 160MHz and 320MHz) in the design are derived from this clock. For the case where the Receiver is configured to receive parallel data, the incoming data are synchronized with the 40MHz clock by the GBT-FPGA, so the Phase Aligner logic is not implemented. For the serial data case at 80Mb/s rate, the incoming 40MHz clock is used in Double Data Rate (DDR) mode to sample the data stream with the correct phase, while for the 160 and 320Mb/s, the incoming 40MHz clock is used to generate the 160 and 320MHz accordingly. Given the finite clocking resources and the delays in the firmware design, a data-to-clock phase alignment is necessary for these two data rates. In order to handle this phase alignment problem, the Phase Aligner was designed to automatically align the data to the center of the data eye.

For this purpose, the Xilinx ISERDESE2 [51] and Xilinx IDELAYE2 [52] primitives are used along with an FSM. The operation of the Phase Aligner is as follows: The incoming 320Mb/s serial stream from the L1DDC (the 320Mb/s case is explained here, a similar process is done for the 160Mb/s case) is driven into two cascaded IDELAYE2 primitives. Each IDELAYE2 is a 31-tap, wraparound delay element with 78ps resolution. The ISERDESE2 is configured as a deserializer, so the serial stream from the IDELAYE2 is sampled with a 320MHz clock with an unknown phase and is converted to 8-bit parallel data synchronized with the fundamental 40MHz clock. The Phase Aligner FSM keeps the E-Link Transmitter in reset state, which results in an output of 0xAA (10101010'b), and the Phase Aligner uses it as

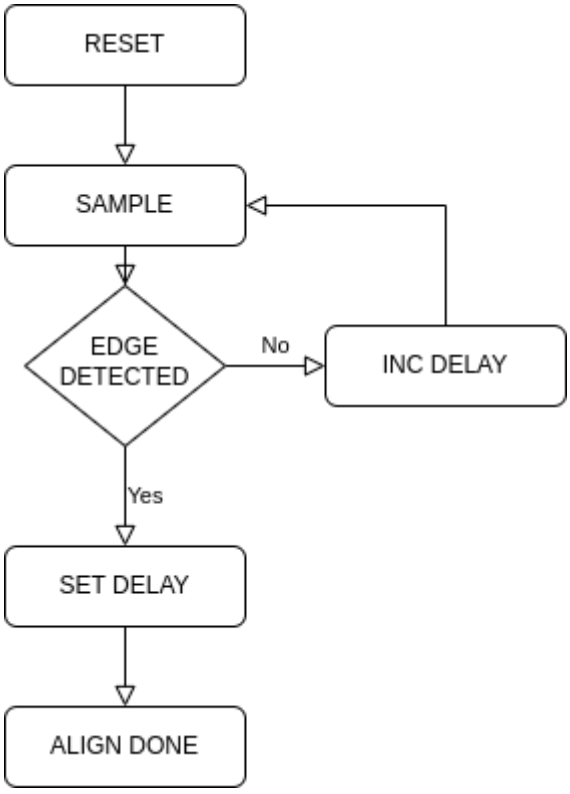


Figure 35: Flow chart of the Phase Alignment FSM states.

a "training pattern." Then, as shown in Figure 35, the FSM takes 256 samples of the 8-bit data from the output of the ISERDESE2 and checks whether all samples are 0xAA or 0x55 (01010101'b which is shifted 0xAA). If yes, the delay is increased by one tap, and the sampling cycle continues. When sampling results in error, at least one sample is not 0xAA or 0x55,

which means that the sampling is done close to the transition edge of the data. Now with a known data-to-clock phase, the FMS decreases the delay by a certain amount (17 taps), so the sampling is done as close as possible to the center of the data eye. After that, the E-Link is declared aligned, and the data are forwarded to the Synchronizer while the E-Link Transmitter's reset is de-asserted.

As discussed previously, the received 8-bits can be shifted by an unknown number of bits for the training pattern; this could be 0xAA or 0x55. An 8-bit synchronization is needed for the actual data to ensure that the 8-bits received match the sent ones. This process is handled by the Synchronizer. The Synchronizer logic consists of shift registers and multiplexers. The incoming 8-bits are stored in a 16-bit shift register clocked by the 40MHz clock. Then concurrently, eight 8-bit copies of the shift register's contents are created, as shown in Table 3, forming the inputs of an eight-to-one multiplexer. The first copy takes the 8 Most Significant Bits (MSB) of the shift register, the second skips the first MSB and takes the next 8-bits, and so on, until at last gets the eight Least Significant Bits (LSB). At the same time, the Synchronizer scans the copies to find the byte 0x7E, which indicates the start of the packet. Once found, the proper select signal of the multiplexer is activated, and the output of the multiplexer is stored to the register with the correct alignment.

Table 3: The eight shifted copies of the incoming data. With green is highlighted the bits that correspond to the start of packet character 0x7E.

16-bit shift register	0111011111100010							
8-bit copies	01110111	11101111	11011111	10111111	01111110	11111100	11110001	11100010
8-bit copies hex	77	EF	DF	BF	7E	FC	F1	E2
MUX select	0	1	2	3	4	5	6	7

The aligned 8-bits are forwarded to the Flag Detector. Subsequently, the Flag Detector receives the 0x7E byte, and if the next byte is not Idle (0xFF), it is interpreted as the start of the packet. Then, the Flag Detector enables the Frame Decoder –Error Detector (FD-ED) and forwards the data. Finally, FD-ED enables the local PRBS generator and compares the incoming data with the generated data for errors. A 16-bit counter is dedicated to this purpose, which increments whenever a comparison error occurs, ultimately evaluating the E-Link performance.

4.2.3 The GBT-SC

The GBT-SC firmware developed by the GBT group completes the functionality of the GBT-FPGA. The GBT-SC is divided into two components: the IC, which implements the IC protocol used for the configuration of the GBTx, and the EC, which implements the SCA channel command protocol over the HDLC protocol handling the communication with the SCA ASIC.

4.2.4 The UDP/IP Ethernet interface

Initially, the L1DDC testing firmware was designed as a stand-alone system. At that time, the only communication with a computer was done through the JTAG interface, where the error

counters and the rest of the monitoring signals were monitored using the Xilinx Integrated Logic Analyzer (ILA). The need for more versatile communication with a computer arose for mass production testing, to provide more debug features, the generation of log files with all measured parameters of the board, and end user-friendliness. A UDP/IP Ethernet interface with a 1Gb/s data rate was added to fulfill those new requirements. The Ethernet Module is divided into two main components; the Slow Control State Machine (SCSM) and the Ethernet interface.

The SCSM acts as a bridge between the Ethernet interface and the GBT-SC and E-Link Interface. It is, in fact, an FSM with many states to be able to: 1) Configure the GBTx of the L1DDC with a pre-determined list of register values, 2) Configure and communicate with the SCA, program the slave GBTxs through the I2C interface, and read the on-board temperatures and voltages using the ADC converter, 3) Interface with the E-Link Interface, readout the error counters, the results of the phase alignment, and other monitoring signals. Since the SCSM firmware was designed to function without the Ethernet communication and subsequently without any software, all the above operations were done purely in firmware. This fact added much more complexity to the design and limited its flexibility, i.e., adding an extra function was a very time-consuming process. Because of the strict schedule of mass production testing, there was no time to redesign this bridge into a more efficient system. Eventually, after the testing finished, the firmware was redesigned entirely and used to test the boards that previously failed the test and retest the boards that were repaired. In this new implementation, only the tasks more efficiently done in firmware were implemented, while the rest of the tasks were handled by the second version of L1DDC testing software.

The UDP/IP stack consists of several components, predominantly Xilinx's Intellectual Properties (IP). As shown in Figure 36, the SCSM communicates via the Advanced eXtensible Interface (AXI) bus with an AXI FIFO [53]. The Ethernet interface reads the data from the FIFO and implements the UDP/IP layers. Then the Xilinx Tri-Mode Ethernet Media Access Control (TEMAC) IP core [54] is used to handle the data link layer, which communicates via the Gigabit Media Independent Interface (GMII) with the 1000BASE-X Physical Coding Sublayer – Physical Medium Attachment (PCS-PMA) IP [55]. The PCS-PMA encodes the data and implements the physical 1000BASE-X standard for fiber optic transmission. The data are then driven to FPGA's GTX transceiver, which serializes them and sends them to the optical SFP+ transceiver. An adapter is used to convert the 1000BASE-X to 1000BASE-T, a copper standard using twisted pair cabling systems, a UTP cable in our case, for the connection with the PC. Since the TEMAC is a product of Xilinx and is not free of charge, an alternative solution was also implemented using an open-source [56] equivalent.

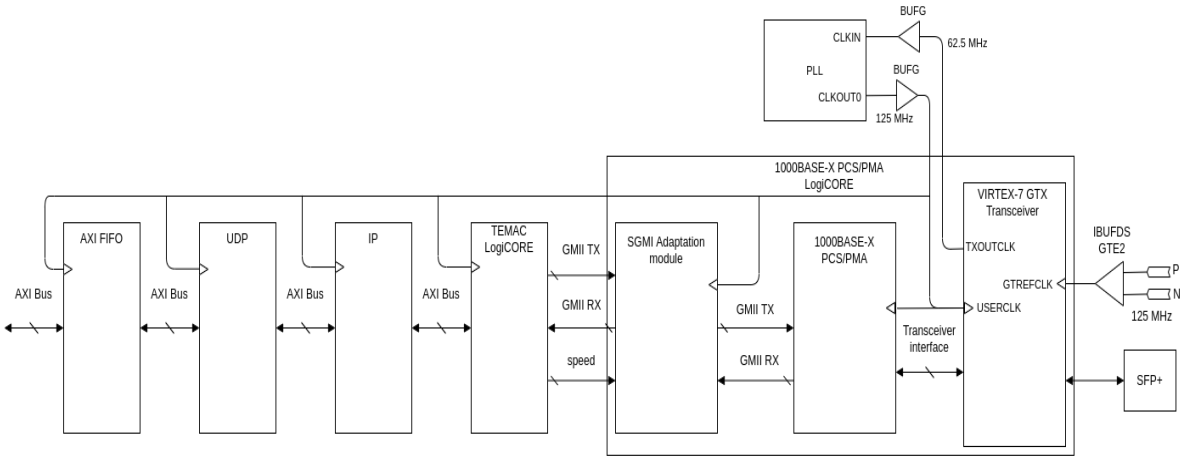


Figure 36: UDP/IP 1000BASE-X Ethernet interface block diagram.

4.3 Software

A fully automated, time-efficient, and user-friendly software (Figure 37) to test the large number of L1DDC boards was developed, named L1DDC Tester. The source code was written in C++ and compiled using the QT Creator Integrated Development Environment (IDE). The working principle of the software is to create requests to the firmware through a Gigabit Ethernet connection in which the firmware responds with its current parameters. The testing process is fully automated and starts by pressing a single button. The first step of the test is to check the optical link stability, then to write/read the configuration registers of the GBTXs to verify that the L1DDC's configuration path is functional and that the registers can be accessed. Afterward, it reads the error counters of the E-Links and SCA's ADC measurements (temperatures of the GBTXs, the temperature of the FEAST DC-DC converters, and their output voltages). The process of readout the error counters and the ADC measurements is repeated every five seconds for half an hour. During that time, if any parameter is above or beyond the specified limits, the test stops with a message showing the name of that parameter. When the testing is completed, a log file containing the status of the performed tests and the unique IDs of the GBTX and SCA is generated.

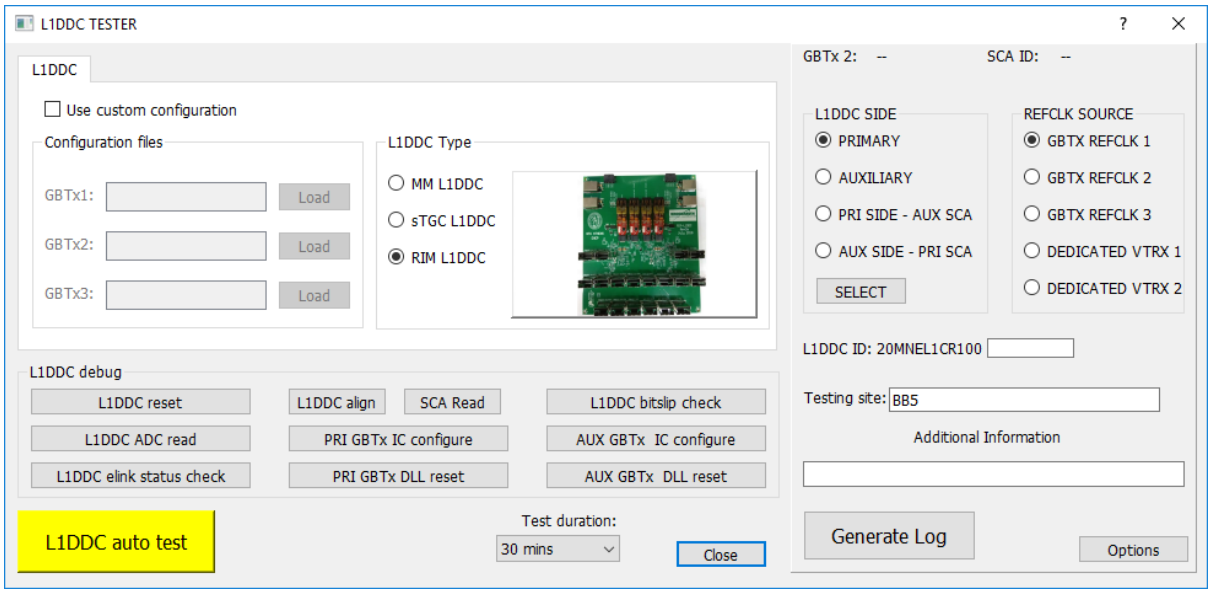


Figure 37: GUI of the Rim-L1DDC testing software.

4.4 L1DDC test results

The performed tests[II] confirmed the bidirectional simultaneous transmission of all electrical and optical signals handled by the L1DDC boards at all supported rates and the intended operation of the GBTX, SCA, and FEAST ASICs. The initial test was a thermal stress screening with ten cycles and temperatures from 0ºC to 60ºC, an eight-hour test to measure the current drain of each card and to check problems with the electrical components. The second phase of the tests was a 30-minute test in which the registers of the GBTXs were reconfigured, bidirectional data were transmitted, and constant monitoring of the voltages and the temperatures was performed. Finally, a small random sample of boards underwent a 24-hour test with data transmission. In total, 572 MM-L1DDCs (522 production and 50 pre-production boards), 572 sTGC-L1DDCs (522 production and 50 pre-production boards), and 40 RIM-

L1DDCs were tested at four identical test stations implemented at University of West Attica (UNIWA), National Kapodistrian University of Athens (NKUA), National Centre of Scientific Research (NCSR) Demokritos, and CERN.

Out of the total L1DDC boards, 32 MM-L1DDC and 35 sTGC-L1DDC failed to pass the tests. So far, nine failed MM-L1DDC and 22 sTGC-L1DDC boards were repaired and passed the test, resulting in a successful yield of 96% for the MMs, 97.7% for the sTGCs, and 100% for the RIM boards.

5.1 Clock Distribution Board

The Clock Distribution Board [I] is part of the NSW off-detector electronics and resides in the Underground Service ATLAS 15 (USA15) area. This board (shown in Figure 38) aims to distribute low-jitter 160MHz clocks to the rim electronics through the Rim-L1DDC. As mentioned earlier, the Rim-L1DDC has two dedicated clock inputs, one for the primary part and one for the auxiliary. In total, 64 160MHz clocks are needed for the NSW (32 Rim-L1DDCs). These clocks will be provided by two clock distribution boards, each with 32 clock outputs. The key component of the board is the Si5345 jitter cleaner made by Silicon Labs. This chip has ten outputs and can generate any combination of output frequencies from any input frequency, with an output range of 8kHz up to 1028MHz. It is fully programmable via SPI or I^2C and features a Non Volatile Memory where the configuration can be stored and recovered during the power-on sequence. The Clock Distribution board consists of four Si5345 chips, three AFBR-811FH1Z optical transmitter miniPODs made by Avago, one Si53306 1:4 fanout chip, and one SR01E12 Ethernet to I^2C module for remote configuration and monitoring of the Si5345 and the miniPODs. The concept of the board is to receive a reference clock from the Atlas Local Trigger Interface (ALTI), then this clock is distributed to the Si5345s through the fanout chip, and finally, the 160 MHz clocks from the Si5345s are driven to the miniPODs. So far, two prototypes of the Clock Distribution boards have been designed. The main difference between them is the input of the reference clock. On the first prototype, two SMA connectors were used to receive an LVDS 40 MHz clock from the ALTI. On the second prototype, the TTC signal from ALTI is used as a reference clock, so the previous scheme was replaced with an FTPDA-R155 optical receiver and an ADN2814 clock data recovery chip which drives the fanout chip.

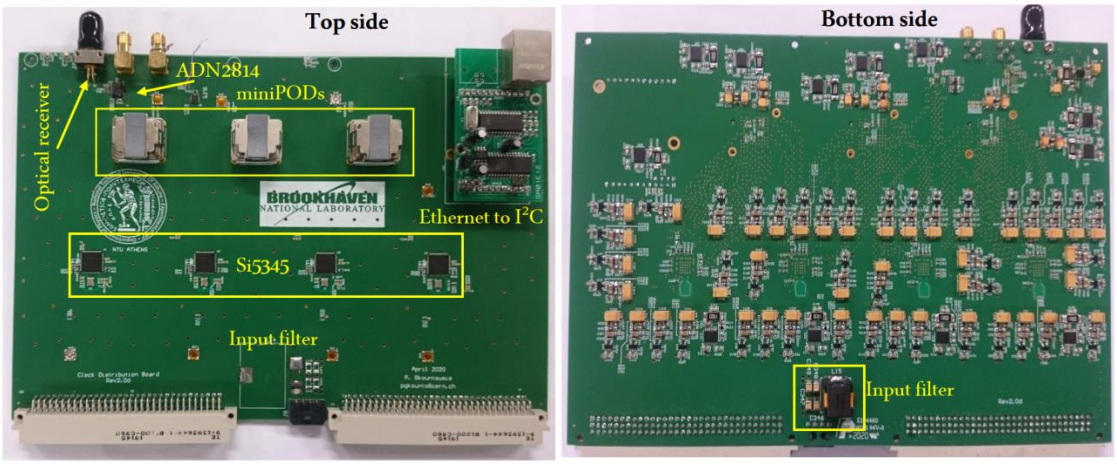


Figure 38: Top and bottom view of the Clock Distribution board.

Both prototypes were assembled manually, and some initial tests were performed. The first test was to measure the output voltages of the 56 on-board LDOs. After this test was completed successfully, the Si5345s were configured. For the configuration of the Si5345, one Si5345 development board was used with a custom-made cable. This method proved unsuccessful since the development board uses 3.3V SPI while the Si5345, by default, is compatible with 1.8V; thus, some registers on the chip have to be modified to switch to 3.3V SPI. A MicroBlaze [57] project was developed on the Xilinx VC709 board to communicate with the Si5345 via 1.8V SPI and modify the registers related to the SPI voltage levels.

Additionally, a GUI was developed (Figure 39) in C++ and with Qt development environment to configure and monitor the Si5345, the miniPODs, and the clock data recovery chip using the on-board Ethernet to I^2C module.

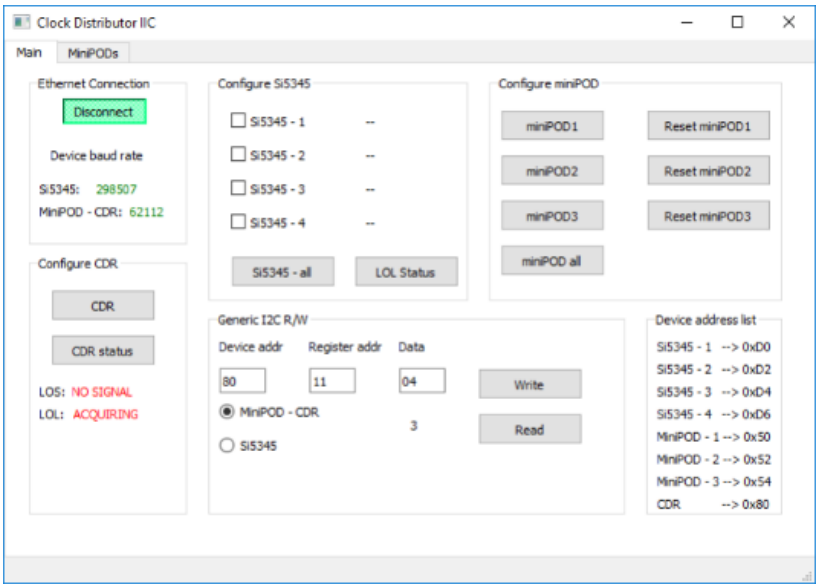


Figure 39: GUI of the Clock Distribution board testing software.

Finally, a test was performed to validate the stability of the output clocks of the board. For this test, the testing setup of the Rim-L1DDC was used along with a set of extra boards and fibers (Figure 40). The functionality of this test is as follows: The Si5345 development board generates the 120MHz reference clock for the transceivers of the VC709 and a 40MHz reference clock for the clock distribution board. Using this reference clock, the clock distribution board generates the 160MHz clocks, which are driven to the miniPODs. From the miniPODs, two of the clocks have to be transmitted to the Rim-L1DDC. For this purpose, a set of different fibers were used. Due to the unavailability of the proper type of fibers, one miniPOD to MTP48 male from a FELIX-712 board was used. The male end of the MTP48 fiber was connected to an MTP-48 female-to-female, and finally, an MTP48 male-to-LC fiber was used to connect with the Rim –L1DDC. In the end, the clocks were verified with a Rim-L1DDC automatic test setup as described in previous chapters.

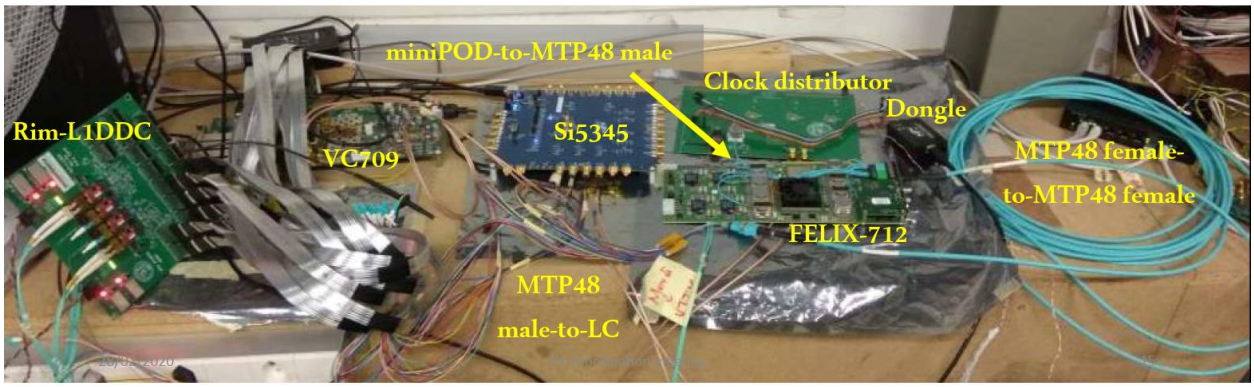


Figure 40: The testing setup of the Clock Distribution board. The setup consists of the Rim-L1DDC testing setup with the Clock Distributor providing the 160 MHz clock.

5.2 LVDS to TTL adapter board

The validation of Micromegas wedges requires testing with cosmic rays where muons are detected. This testing takes place on a facility named Cosmic Ray Stand (CRS) using a set of scintillators that provide the necessary trigger signals, effectively emulating the functionality of the sTGCs. These trigger signals must be aligned with the leading edge of the emulated 40MHz bunch crossing clock. A set of different modules is used to align these two signals, as shown in the block diagram (Figure 41) below. In this scheme, the Nuclear Instrumentation Module (NIM) logic level trigger signal from scintillators is driven to the Clock and Trigger Fan-out (CTF) module, where it is converted to CML 1.2V logic standard. Then, it is driven to the VC709 development board through miniSAS Twinax cables along with the 40MHz clock from one L1DDC.

The firmware of the VC709's FPGA synchronizes the trigger pulse with the clock, and the output is driven to the LVDS-to-TTL board through coaxial SMA cables. Finally, the TTL output of the LVDS-to-TTL board is fed to the TTL-to-NIM module to convert the fine trigger signal into the NIM standard.

To complete this chain of modules and boards, an LVDS-to-TLL board was designed in the framework of this thesis. The LDVS-to-TTL board features one dual DS90C402 LVDS receiver made by Texas Instruments. For the input side of the receiver, SMA connectors were used to make the connection with the VC709 easier, and LEMO connectors were used for its output to be compatible with the TLL-to-NIM module. So far, one such board has been fabricated and used at the Micromegas CRS.

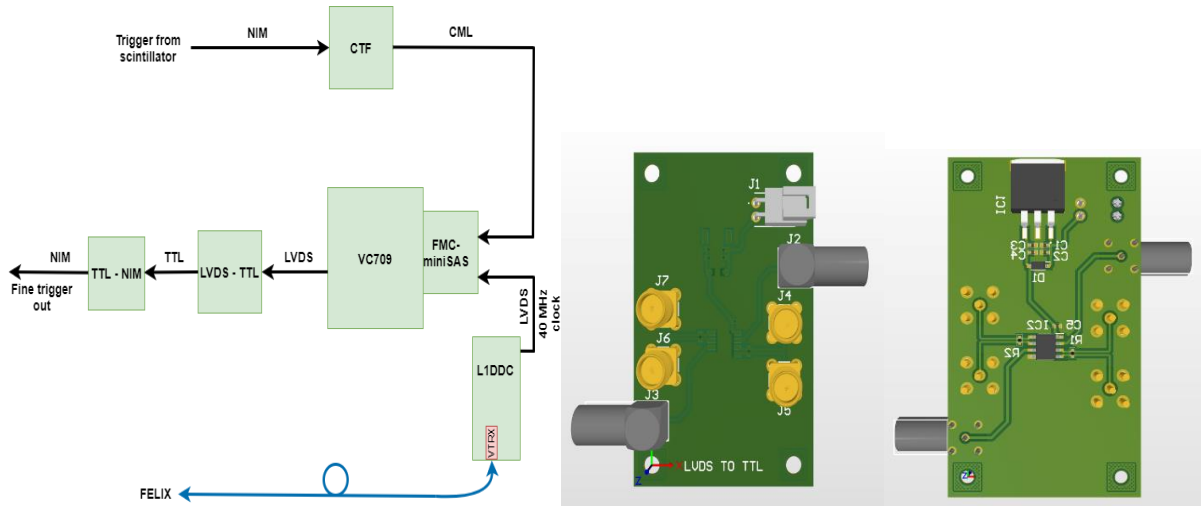


Figure 41: Left: Block diagram of the fine trigger system. Right: 3D model of the LVDS to TTL board.

5.3 Differential Safety Mechanism

The New Small Wheel (NSW) Micromegas detector wedges for ATLAS experiment upgrade at CERNduring their integration pass from different sequential installations and QA/QC procedures, while a final performance operation test is performed in a Cosmic Ray Stand (CRS). In this test the two single wedges, that constitutes a double wedge, is a complete detector to be installed to the NSW detector system at CERN. The protection of the wedges against an unexpected gauge pressure increase at their operation test at CRS and also at their final position at NSW is essential. Because the gauge pressure inside the volume of the Micromegas volumes is not feasible, the only way to sense an unexpected pressure growing is to use an intelligent mechanism acting with an indirect way by sensing the growing of the static gauge pressure in the input gas line. We must note that a bubbler or a passive safety valve is

improper for this purpose, as we explain in the next section. The detector wedges are designed to operate at low static gauge pressure, around 3 mbar, with an upper typical limit of 10 mbar. Higher pressures must be avoided due to deformations caused by volume expansion and the subsequent risks for damage. In the present work we describe the design and implementation a "Differential Safety Mechanism" (DSM) [III][IV] for protecting the detector wedges against unexpected and sudden increasing of the static gauge pressure inside its volume. This is achieved in a indirect way by sensing the sudden growing of the inlet gauge pressure in the gas line. The DSM is essentially an asynchronous digital sequential system based on a adjustable voltage comparator and other digital logic circuits for driving a 3-way solenoid valve at the correct time interrupting the pressure growing and releasing the wedges to 40 the atmosphere.

5.3.1 The basic idea and motivation

During the final performance operation of the wedges at CRS there is finite probability of static gauge pressure sudden increase due to several unexpected reasons. The most likely one is the blocking the intermediate part of the output gas line by accident by human action. In Figure 42(left) the location of the DSM at the input gas line, at the point is shown. The risky gas line part for blocking is the A2A3. If this happens, the static pressure in this line and that inside the wedges IP and HO tend to be equalized converging rapidly to the level of the gas mixer output, that is, around 1 bar. Because the location of the blocking point is unknown, we are forced to put the safety mechanism before the wedges, at the pointA1. On the other hand, the maximum allowed static gauge pressure in the wedge, around 10 mbar, ismuch lower than that in the input gas line (in the region of point A1 due to the installed gas impedances in both sides of the two wedges. For this reasons an appropriate mechanism must sense the growing ofthe pressure by a predefined amount, that is, to operate differentially. Based on this idea, the "heart" of the DSM is a voltage comparator by using OPAMP in which the reference voltage level is adjustable.The comparator gives a digital voltage signal (command) for activating a 3-way solenoid valve, normallyopen. This valve can perform two functions at the same time: a) gas release from the wedges and b)interruption of the input line. The timing diagram of the DSM operation cycle is given in Figure 42 (right). Other needed functions are also included and are described next.

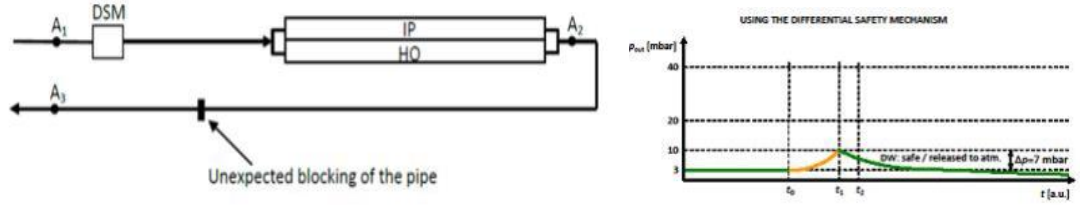


Figure 42: Left: The location of the DSM in the gas input line of a single wedge and the hypothetical blocking point in the gas exhaust line A2A3. In this situation the wedges should be completely damaged in a few seconds. Right: Diagram showing the operationof the DSM. Assumed a blocking at timet0, the pressure starts to increase until the predefined limit for DSM activation at time t1.

5.3.2 DSM operation

The main circuit of the DSM mechanism is a comparator driving a Flip-Flop. The sensing of the pressure increase is done be a high precision differential pressure transducer, type 144LP50D-PCB, from FirstSensor, while the voltage difference can activate the 3-way

normally open solenoid valve, type VLV11-10-4-BV-5P88 . In the electronic schematic, given in Figure 43, we can see the location of the voltage comparator, the driven J-K Flip-Flop which, in turn, provides the activation command to the solenoid valves (in the case of using two 1-way solenoid valves). Moreover, there are also buttons for test and reset operation. In the final design we used a 3-way normally open solenoid valve. During the normal operation of the Micromegas wedges we provide gas at a nominal flow rate which some times is adjusted manually in lower or higher level, At any flow rate the static gauge pressure in the input is developed due to the "external impedances" of each wedge by a non-linear way. The relationship between the flow rate and the static pressure is known and therefore, in any selected flow rate we expect a corresponding value of the nominal static pressure. The differential pressure transducer (DPT) we use in the DSM has a full scale 0-50 mbar with an output voltage in the range 0-5 V leading to a pressure to voltage conversion factor equal to 0.1 V/mbar. For a typical nominal static pressure corresponds a voltage output of the DPT which we call "Threshold Voltage", VTR. In order to set a tolerance above the nominal static pressure (and thus in voltage) as a critical acceptance limit we define that voltage that we call "Reference Voltage", VREF, which corresponds to a static pressure 7 mbar above the nominal one. This value comes from the maximum allowed static pressure in a wedge, 10 mbar, included the typical pressure in the output due to the bubbler, which is around 3 mbar. Therefore, the pressure difference for sensing any sudden blocking of the gas line is 10-3=7 mbar. The reference voltage is calculated as folows: VREF = 5(pnom/50) + 5(7/50) = 0.1(pnom +7) V. For a typical flow rate of about 17 L/h (reading in a rotameter 20 L/h) which corresponds to pnom = 25 mbar we obtain VREF = 3.2 V. Below we give the list of the functional features of DSM.

- The mechanism is activated when the If VTR > VREF, setting valve 1 to OFF (closed) and the valve 2 ON (open). Both solenoid valves remain in this state until the RST (reset) button is pressed (the red LED becomes ON) under the condition that the static pressure has been lowered by at least 2 mbar. In this state, the gas line closes, and the Detector Chamber diverges to the atmosphere from its input.
- If happens electric power cut, the gas continues flowing but the mechanism is not in the standby state (the green LED is still ON).
- By pressing the test button, we can verify the activation functionality of the mechanism.
- The reference voltage VREF can be set by the potentiometer; while measuring the pressure sensor voltage we can monitor the set reference voltage.
- Two LED, red for the activation and green for the standby state are used.

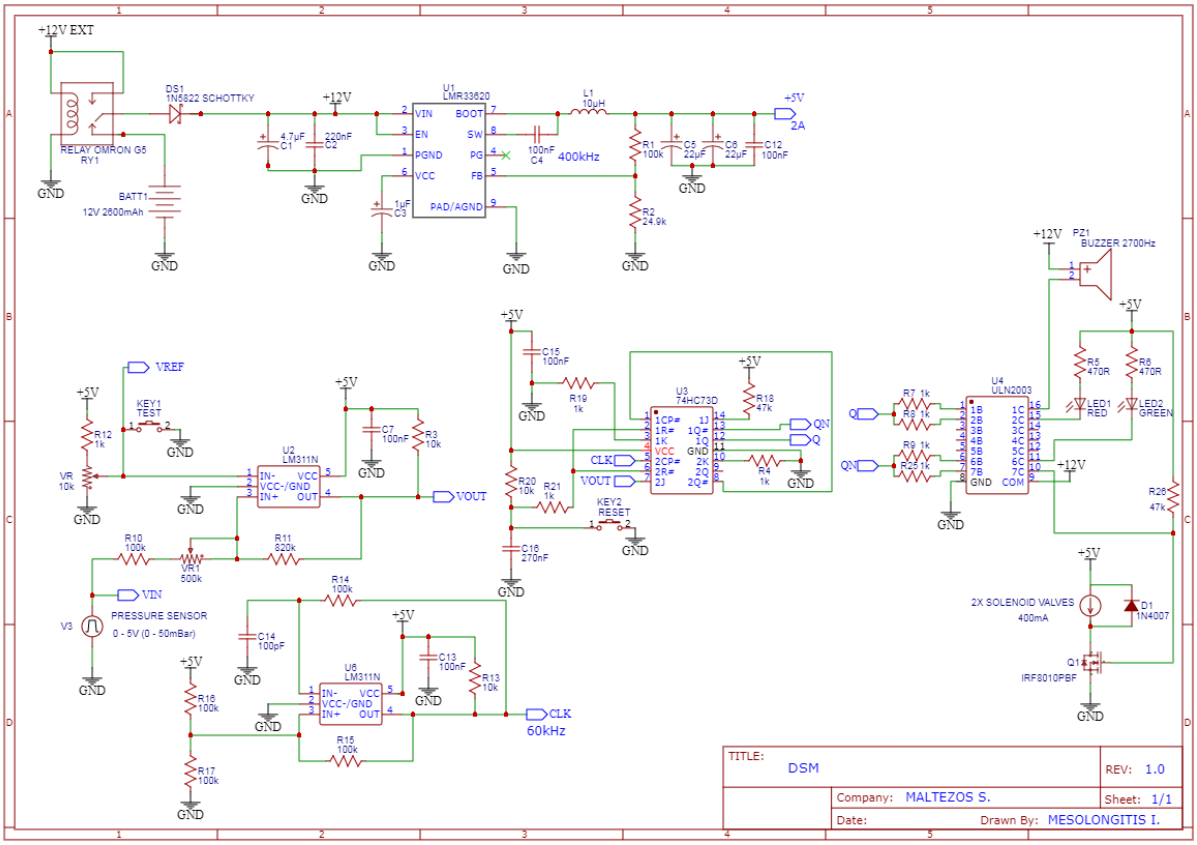


Figure 43: DSM schematic drawing.

5.3.3 Simulations and measurements

During its design simulations were performed for optimizing the performance of the operation. The main functionality was tested by using PSpice. The schematic and the resulting plots are shown in Figure 44 and Figure 45. The simulated circuit included the two comparators, the two J-K Flip-Flops, and the low-side switching circuit. The corresponding electronic schematic is given in Figure 44. To simulate the output signal of the pressure transducer a triangular-shape periodic pulse was utilized. When the voltage exceeds the reference one (2 V) the output of the comparator drops to zero driving the logic level of output of the Flip-Flop to rise at high level (5 V). This voltage level remains constant and via current drivers deactivate and open the one gas port of the solenoid valve (which is normal closed) and at the same time activate and close the other gas port (which is normal closed). Therefore, the Micromegas wedge are released to the atmosphere while the gas input line is blocked stopping to provide gas.

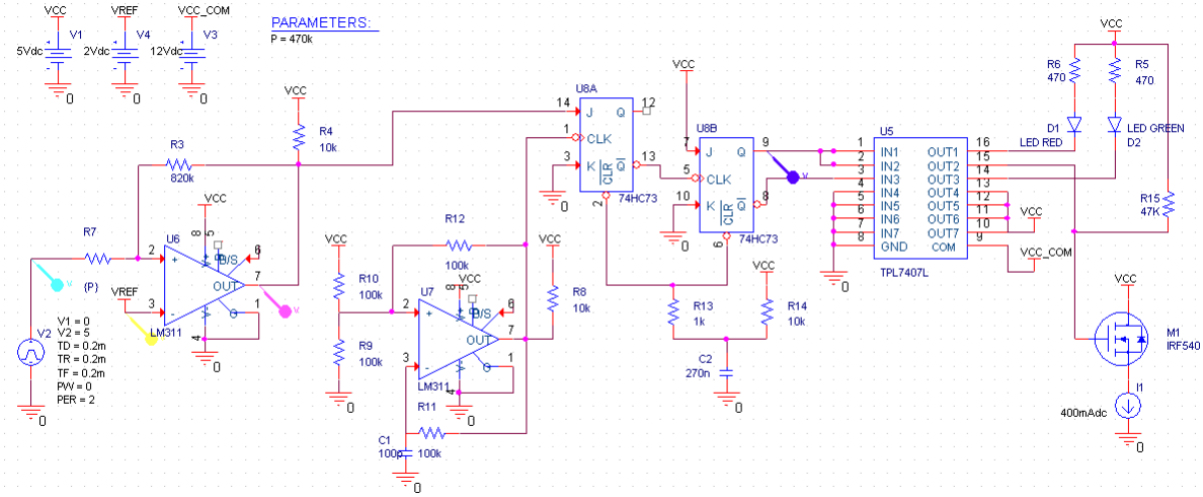


Figure 44: The schematic used for the PSpice simulation.

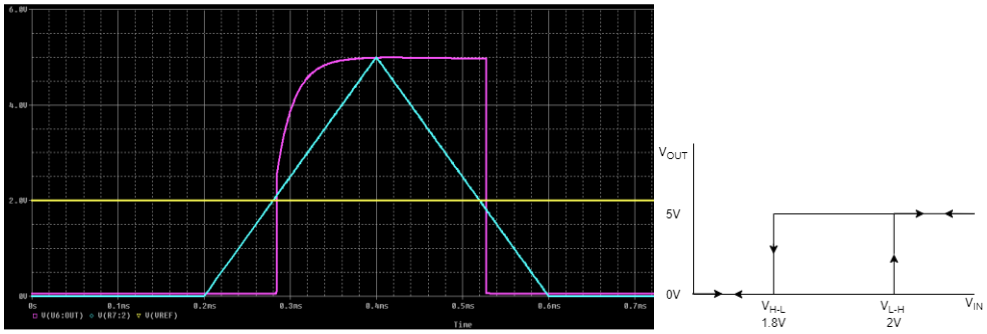


Figure 45: Left: The PSpice simulation waveforms. Right: The hysteresis curve.

Finally, when the first prototype was fabricated, it was tested with a signal generator that produced the same triangular pulse like the one in the simulation. An oscilloscope with three probes was used to measure the voltages of the generator output (pressure sensor), the threshold voltage and the output of the comparator. As shown in the Figure 46, the behavior of the circuit is the expected and identical to the simulation.

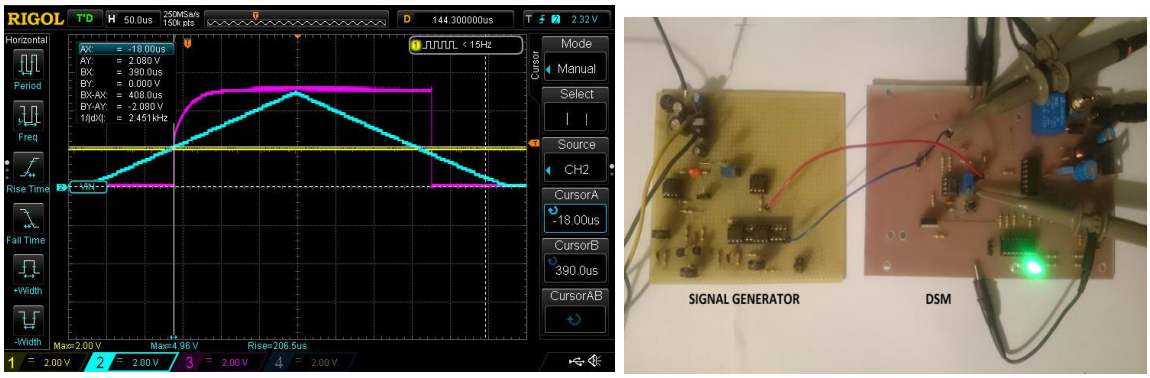


Figure 46. Left: Oscilloscope screenshot showing the input signal(blue), the threshold of the comparator (yellow), and the output of the comparator (magenta). All the waveforms are consistent with the ones from the simulation. Right: the test setup showing a handmade signal generator and the DSM prototype.

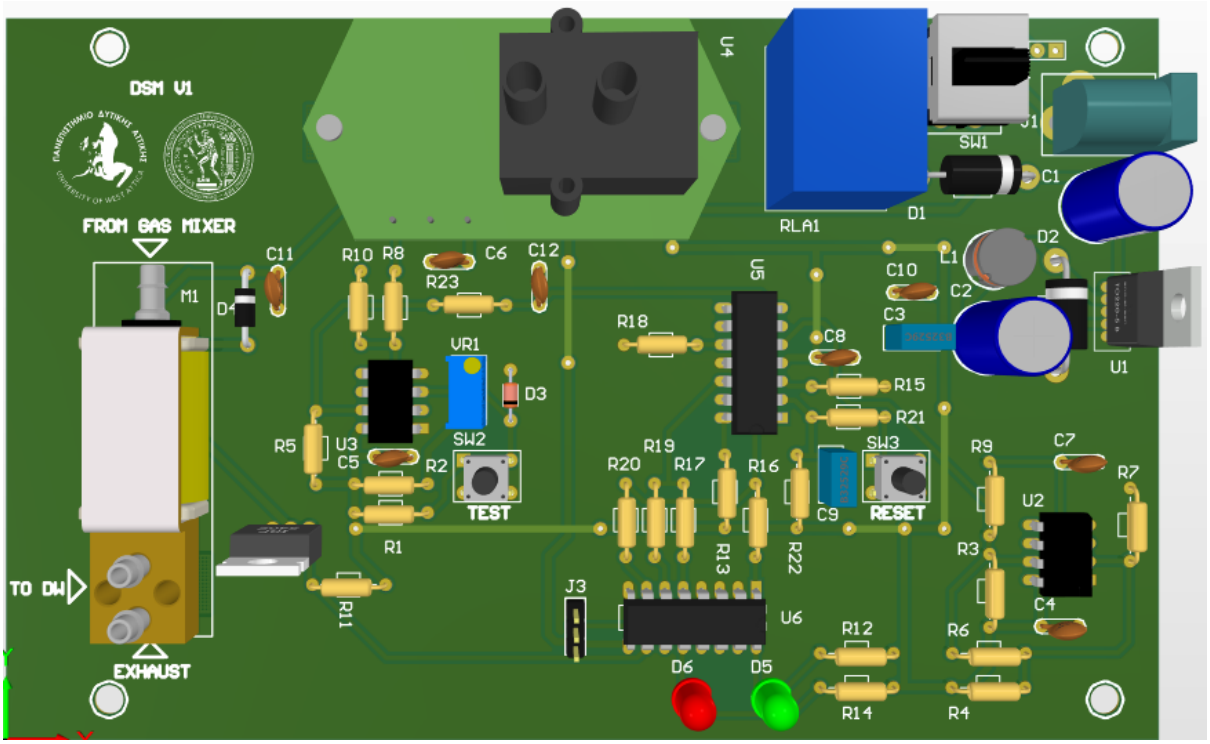


Figure 47: 3D model of the DSM, created with ALTIUM.

5.4 NSW Noise Investigation

From the early beginning of the MM sectors' integration tests, noise issues became evident. The noise problems worsened when the sectors were installed on the NSW wheel. Subsequently, identifying the noise sources, the electromagnetic immunity of the detector and the possible solutions became a priority of the NSW project. In this section, one year's work is presented, performed by the author, Professor T. Alexopoulos (NTUA), and G. Iakovidis (Brookhaven National Laboratory, USA). During that year, several noise sources were identified and suppressed, and the grounding scheme of the detector was improved, providing the best possible noise reduction.

It is worth mentioning that the noise problem was critical to be solved urgently for the NSW detectors to be installed on the chassis on time. Therefore, the management of the NSW project decided to establish a Noise Task Force to address that challenging issue.

In the framework of this thesis, the identification of the primary noise source and the noise solutions were intensely debated in the weekly Task Force meetings, discussed among the nominated experts, underwent further tests, and finally, they were accepted by the Noise Task Force as the best possible for the noise challenge.

This section is divided into three subsections that correspond to the noise sources and extensively describe the mitigations performed to reduce the noise.

5.4.1 The ADDC noise and mitigation

The ADDC board, as discussed briefly in section 1.3, is an on-detector board handling the trigger signals of the MM detectors. This board has 2 GBTxs, two ART ASICs, one SCA, two FEASTs, and one VTTX. 16 ADDC boards are used in every MM sector. Analyzing the noise baseline plots from the MM sectors, it was revealed that there were noise peaks in the vicinity

of the ADDC boards. An investigation started to find out whether the ADDC is the noise source and, if so, what it is causing it. Besides the noise baselines from the readout, the VMM has an output named monitor output, which, when configured, outputs the analog signal of one of the 64 VMM channels. The monitor output in the MMFE8 board that hosts the VMMs is connected to an MMCX connector which can be connected to an oscilloscope to monitor one of the detector's strips in real-time. That monitor output signal was one of the main tools we had to track and analyze the type of noise as "seen" by the detector, apart from the noise baselines.

By analyzing the noise picked up by the detector through the monitor output, it was observed that the noise's frequency was 1.2MHz. This frequency was verified that has the same value as the frequency the FEAST DC-DC converter is switching. To prove this, a home-made magnetic loop antenna of 1cm was constructed using a coaxial cable. The antenna was also connected to a different oscilloscope channel, which monitors the monitor output signal. By bringing the antenna close to the one FEAST of the ADDC and triggering the oscilloscope to the monitor output, it was visible that the two signals were correlated, proving that the noise sources were indeed the ADDC's FEASTs. All the on-detector electronics use the FEAST for their DC-DC converters, and all of them use shields to avoid EMI, but only the ADDC ones generated noise. By comparing the layout design of the ADDC with that of the L1DDC or of the MMFE8, it was clearly visible that the L1DDC (and the MMFE8) has multiple via in the perimeter of the FEAST layout while the ADDC has none, as shown in Figure 48. Those vias are very important and act as the continuation of the shielding from the top layer of the PCB to the bottom. Without those vias, the EMI escapes through the internal layers of the ADDC PCB, thus inducing noise in the detector.

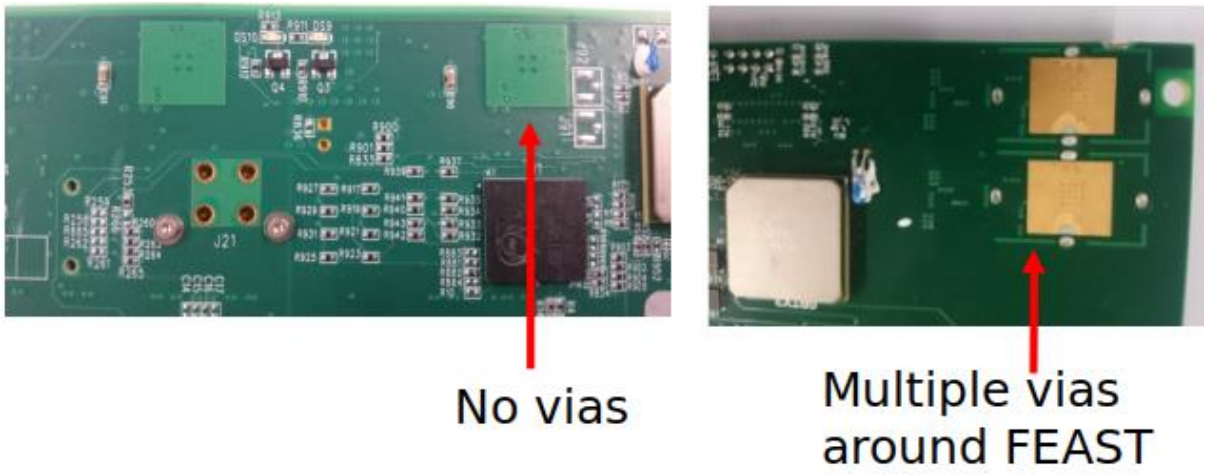


Figure 48: Comparison of the ADDC(left) and L1DDC(right) FEAST layout.

After that design error was found, the only feasible solution was to make a Faraday cage to enclose the board, minimizing the EMI. This approach was not very easy to implement since the Faraday cage interferes with components on the detector, components on the ADDC, and the mounting holes and stand-offs of the board, to name a few. Despite those difficulties, the Faraday cage solution effectively eliminated the noise issue. A noise baseline comparison of with and without the cages is shown in Figure 49.

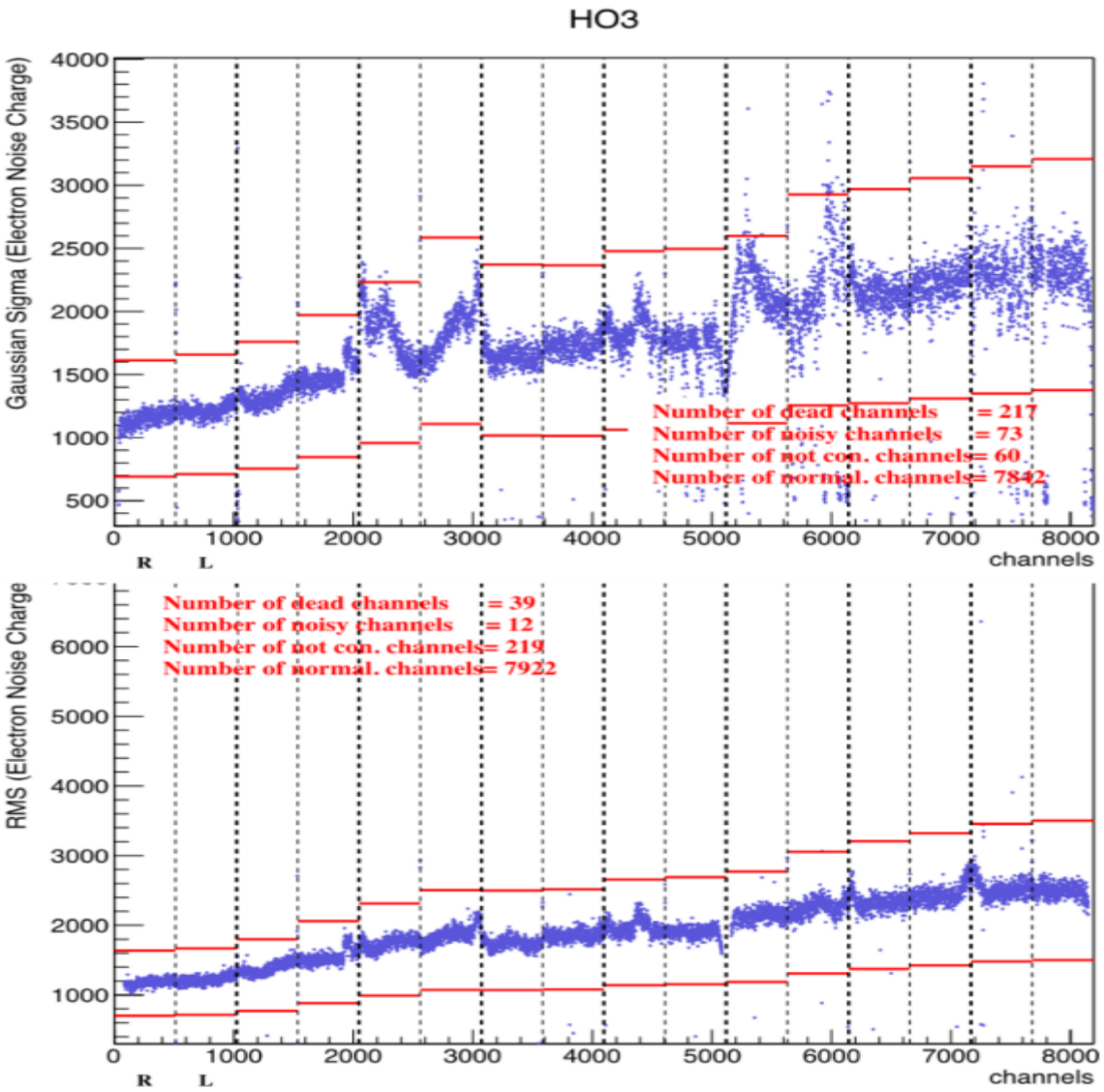


Figure 49: Noise baseline plots. The top one is without the Faraday cage, and the bottom with it. The vertical axis is the RMS noise expressed in electrons, and the horizontal is the VMM channels of the eight PCBS of one MM layer.

More than ten prototype copper cages were made by hand and tested for their effectiveness to find the best Faraday cage solution; a few are shown in Figure 50.

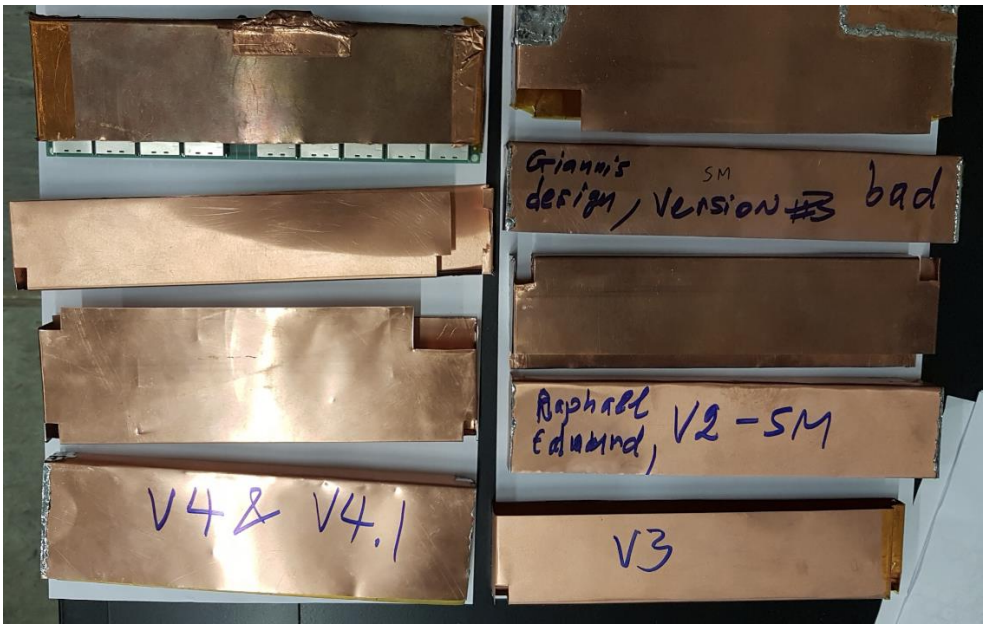


Figure 50: Some of the Faraday cages prototypes. The one marked as V3 is the final design.

The final design is illustrated in Figure 51. The cage has two holes in the backside for mounting clips and a step-like structure to make room for an HV capacitor on the detector. A Kapton layer is placed inside the cage to avoid short circuits with the interfering components, and a graphite thermal pad was added to the bottom to improve thermal conductivity and avoid galvanic corrosion between the copper cage and the aluminum detector structure.

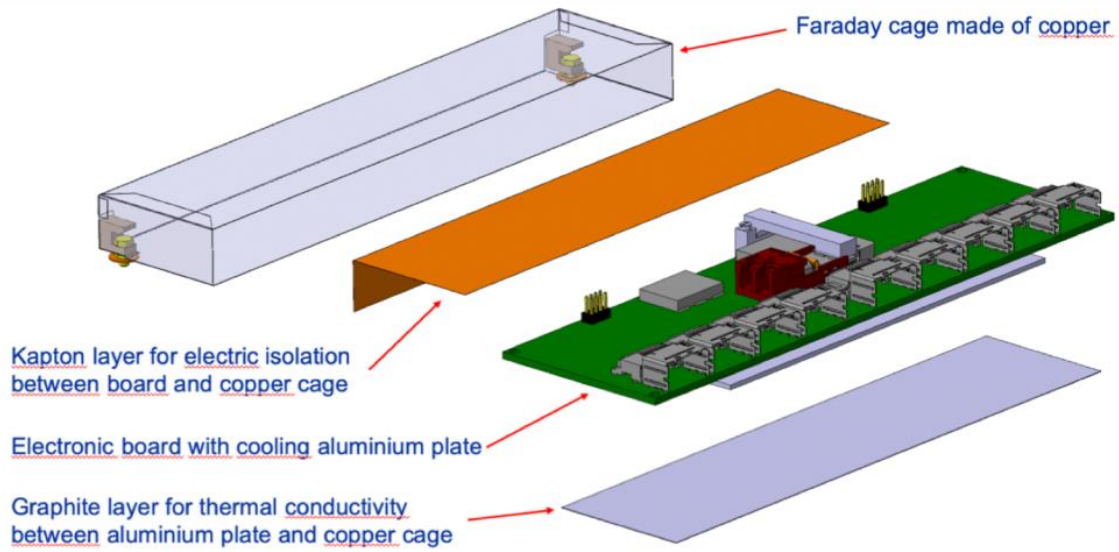


Figure 51: A 3D model of the Faraday cage assembly with the Kapton layer on top of the board and the graphite cooling pad at the bottom.

Since the ADDC noise problem was an unforeseen issue, many already completed sectors had to be removed from the NSW wheel and refurbished with the Faraday cages, causing logistical and scheduling issues for the project. The design of the cages was handed to a company to fabricate the 570 cages needed as fast as possible. Even with the best-estimated

delivery time from the company, it would take several months to deliver the first batch creating an even bigger scheduling problem.

To begin the refurbishment as quickly as possible, we proposed voluntarily that the author could take the responsibility of fabricating some cages by hand until the company delivers the rest. Since the company failed to deliver the cages on time, 180 were fabricated by hand and tested for their efficiency in reducing the noise, enough for 11 Micromegas sectors of the NSW. In addition, the company could not solder the cages' seams and intended to hand the task to a separate company that charged 50CHF per cage. To save expenses and valuable time, the remaining 370 cages were soldered by hand and tested for their efficiency in reducing noise well ahead of schedule.

5.4.2 The MM detector's grounding scheme mitigations

The grounding scheme is a significant factor in any electronic system's noise immunity. That becomes even more important for particle detectors because of their low signal.

The grounding scheme of the MM detectors consists of the spacer frame (Figure 76 in the Appendix), that is the aluminum chassis on both sides of which the MM detectors are situated, as shown in Figure 52, connected in both longitudinal edges with the metal chassis of the NSW via 0.5cm diameter ground cables.

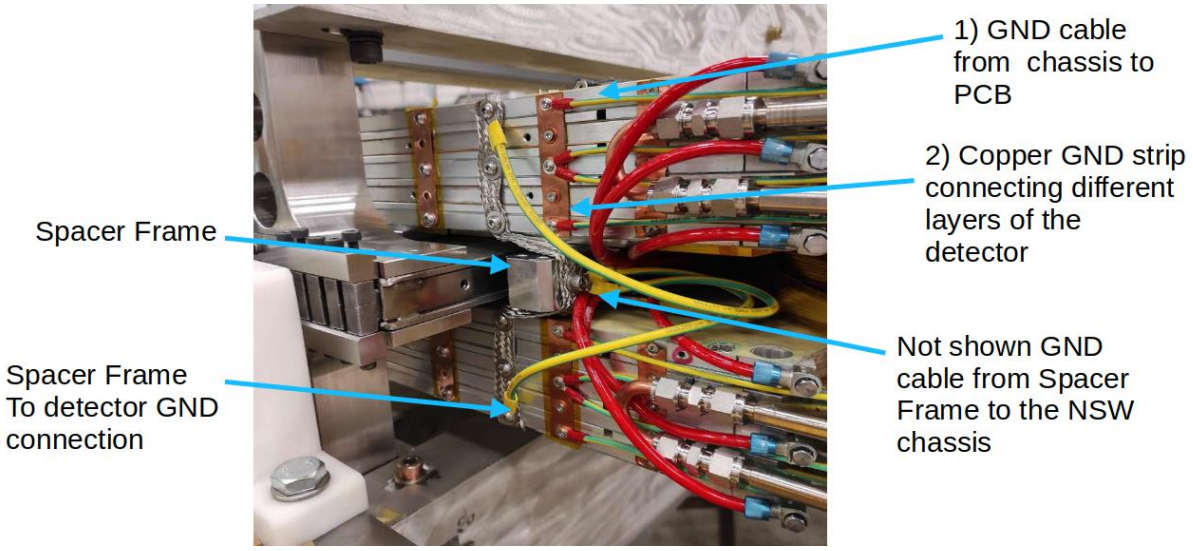


Figure 52: The ground connection of the MM detector, one of the four corners, is pictured.

To improve the grounding of the detector, thicker ground cables (marked as 1 in Figure 52) were used to connect the chassis with the PCBs of the detector. Additionally, the Copper-Kapton ground strips were replaced with handmade 0.2mm thick copper strips (marked as 2 in Figure 52) since the Copper–Kapton strips were easily deformed and provided poor electrical contact with the chassis, as shown in Figure 53.

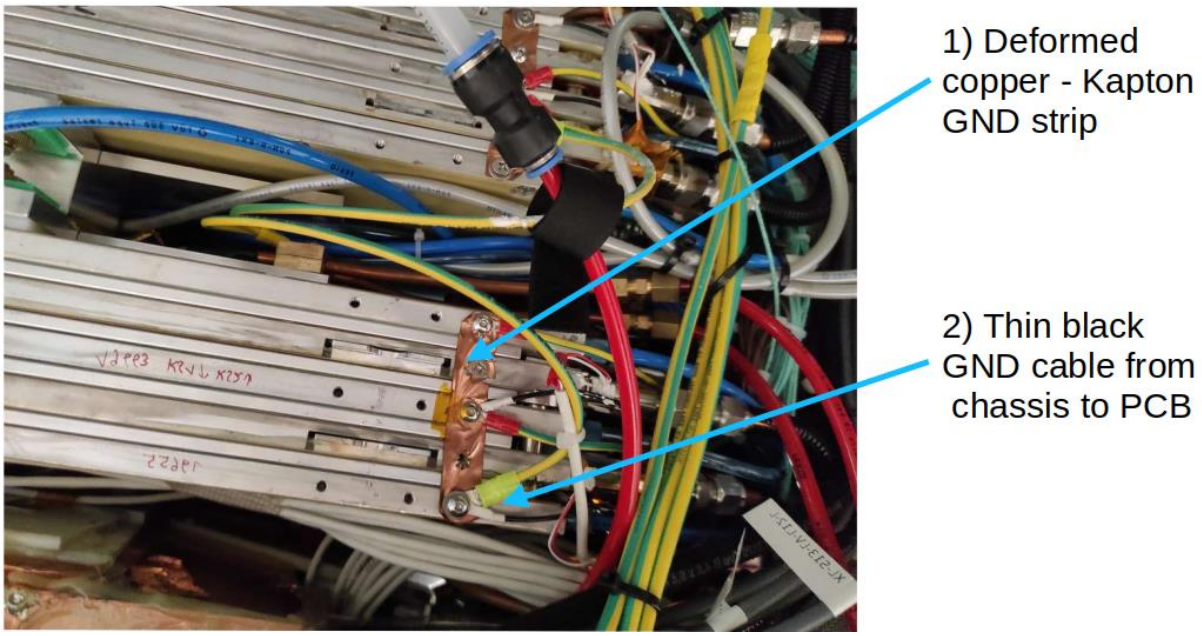


Figure 53: The original grounding, consisting of Copper–Kapton GND strips and thin wires.

These modifications had a consistently positive impact on the noise levels of every MM sector. A comparison of the noise levels before and after the modifications is shown in Figure 54.

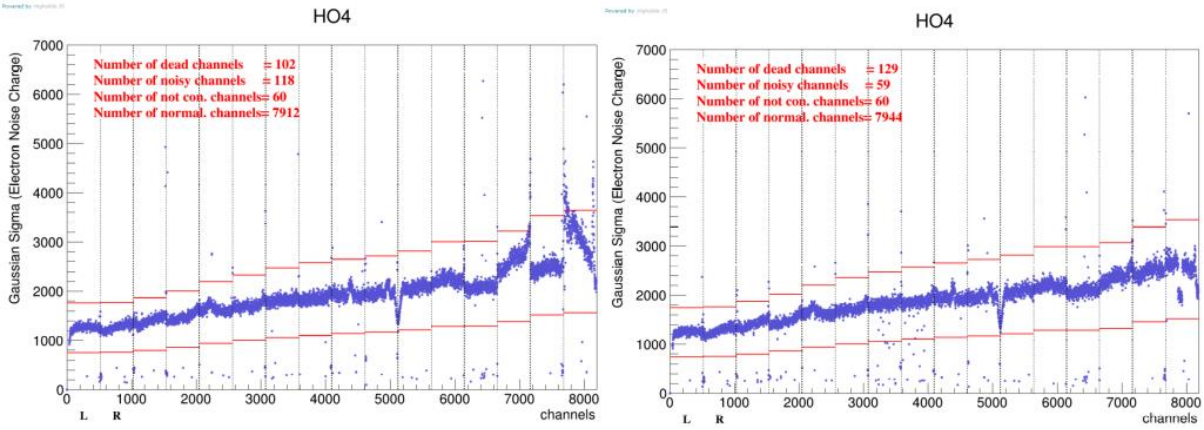


Figure 54: Noise baseline comparison: Left: the noise level with the original grounding scheme. Right: with the improved cabling solid copper GND strips.

Although the above modifications improved noise, there were regions of the detector that still had high noise levels. To fix that, additional ground cables or copper braids were placed from these regions to the spacer frame, but the results of these modifications were inconsistent; sometimes improvement was observed, other times no change was detected, and sometimes the noise level even worsened. So, the extra ground connections in regions that were not initially designed for grounding provided a not trustworthy solution. The most reasonable explanation is that these extra connections created ground loops and redistributed the noise across the detector.

An explanation of weak noise spots in the detector could be that there are many choke points in the ground plane of the PCBs and weak connections between different PCBs, as shown in Figure 55.

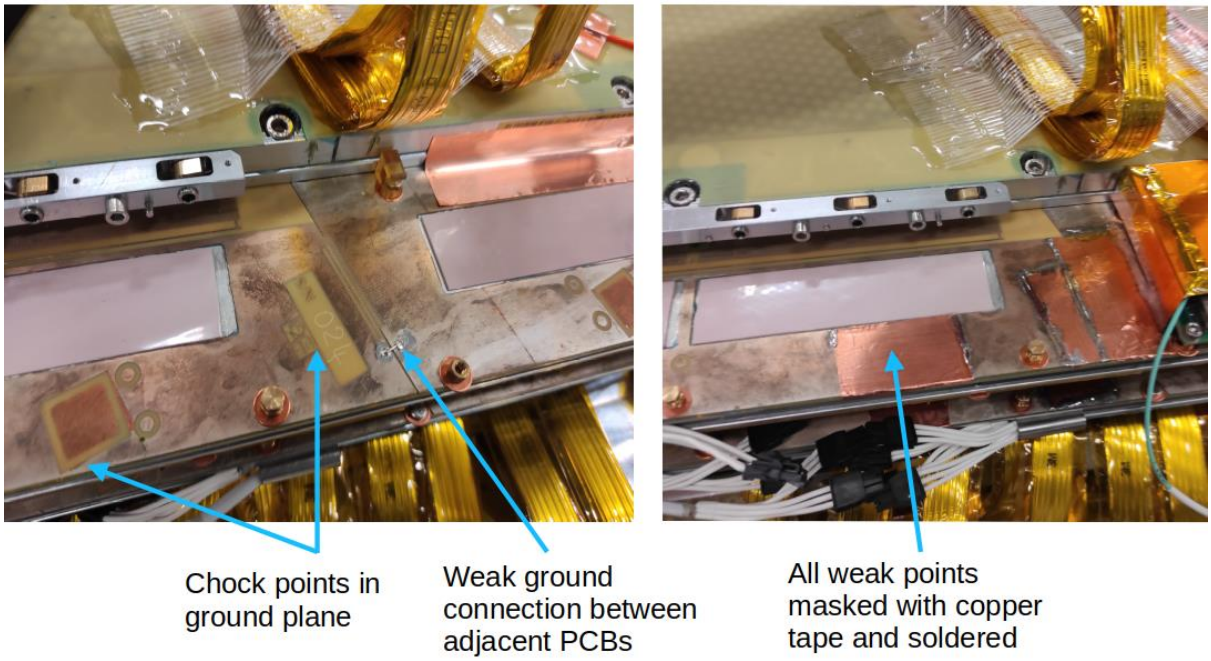


Figure 55: Left: choke point of the detector's ground plane. Right: the same location with the weak points masked with copper tape.

An effort was made to prove this point by masking hundreds of weak ground points of a MM sector with soldered copper tape. The result indeed proved that if the detector's PCBs were designed without these weak points, the noise would be satisfactory, eliminating the need for additional ground cables.

Although the positive results of the above solution, it was not feasible to perform such modifications in all sectors since it would require many days to accomplish, and the copper tape soldering should be performed very carefully so it interferes as least as possible with the cooling pad of the boards.

With this mitigation unable to be implemented in all sectors, and even in the sector with the mitigation done, the noise levels were still high. Therefore, it was evident that something else was inducing noise in the detector. In the search for the noise source, we kept applying the grounding modifications mentioned before, but the focus was turned toward eliminating the noise sources.

To underline how important it had become, for the NSW collaboration, to solve the noise problem, it is worthwhile mentioning that other groups working on the project claimed ownership of the solution described above.

The follow-up of the hunt for the noise source is described in the following subsection.

5.4.3 The Intermediate Converter Stage (ICS) power supply noise and modification

In the search for possible noise sources, a large magnetic loop antenna was made of scrap copper wire (Figure 56). This simple and costless tool proved the key to solving the NSW noise problems.

Figure 56: The magnetic loop antenna used in the noise investigation. The antenna is wrapped in Kapton tape and has a BNC connector for being connected to the oscilloscope.

Many noise sources were identified by using the antenna, such as Switch Mode Power Supplies (SMPS) powering equipment in the vicinity of the detector, unshielded cables, and heavy electrical equipment in the basement of the building where the testing of the MM sectors took place.

The breakthrough, though, was the revelation that the Intermediate Converter Stage (ICS) power supply designed to power all the on-detector electronics emitted a tremendous amount of noise. To prove that the ICS' noise was indeed present in the noise waveform of the detector, an oscilloscope was used to monitor the MMFE8's monitor output and the signal from the antenna placed on the ICS crate, as shown in Figure 57.

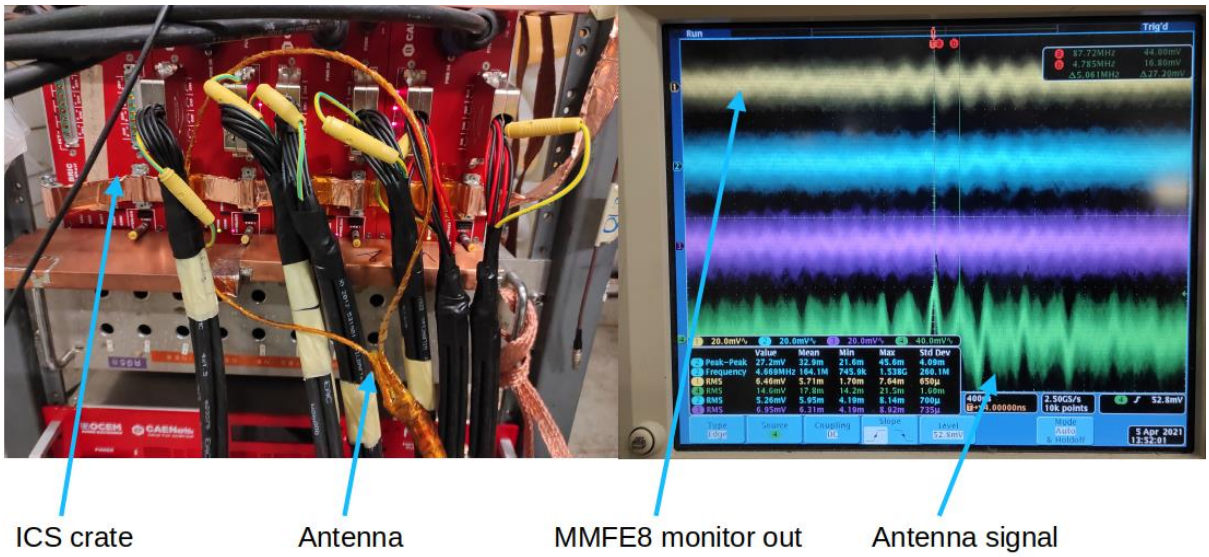


Figure 57: Left: the loop antenna close to the ICS. Right: The correlation of the noise picked up by the detector and the antenna.

As shown in Figure 57, the noise picked up by the antenna correlates with the noise picked up by the detector. The fundamental frequency component of the ICS noise is around 5MHz, (a screenshot (Figure 78) from a spectrum analyzer is available in the figures appendix), providing a strong argument that the noise comes from the ICS. Indeed, after disassembling the ICS, it was revealed that the ground plane layout of the ICS's front panel was poorly designed: as shown in Figure 58, there were small ground loops close to the output connectors, zero-Ohm through-hole resistors were used to connect the ground planes, and the ground plane resembled more a trace with narrow points than a solid ground plane.

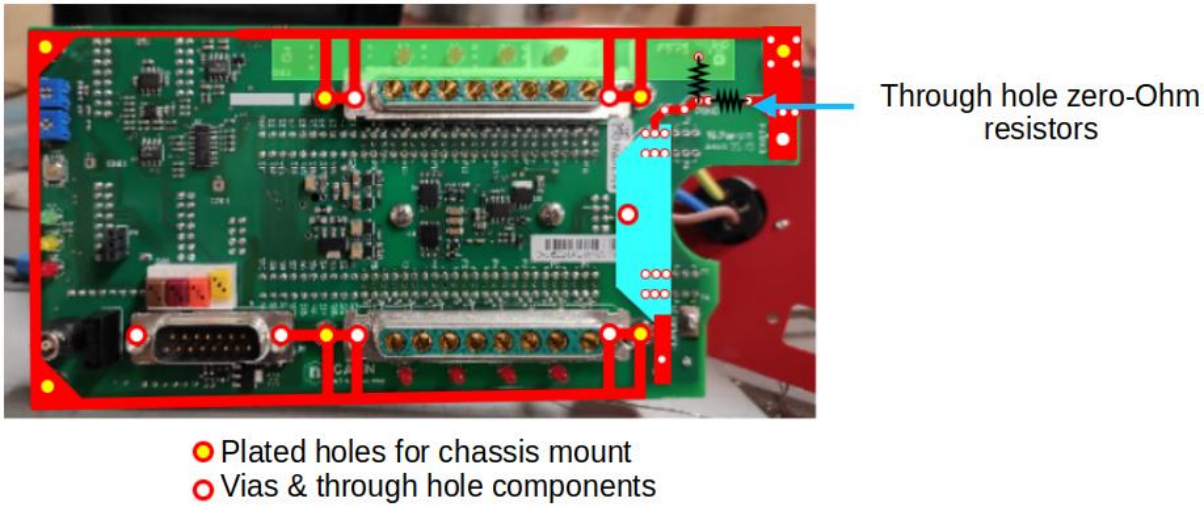


Figure 58: Reverse-engineered ICS ground plane connections.

Additionally, measurements were taken at the output pins of the ICS between the plus and ground and between the minus and ground. As shown in

Figure 59, the noise level is unacceptably high, around 10mV RMS (noise level up to 100mV peak-to–peak was measured in other ICS channels).

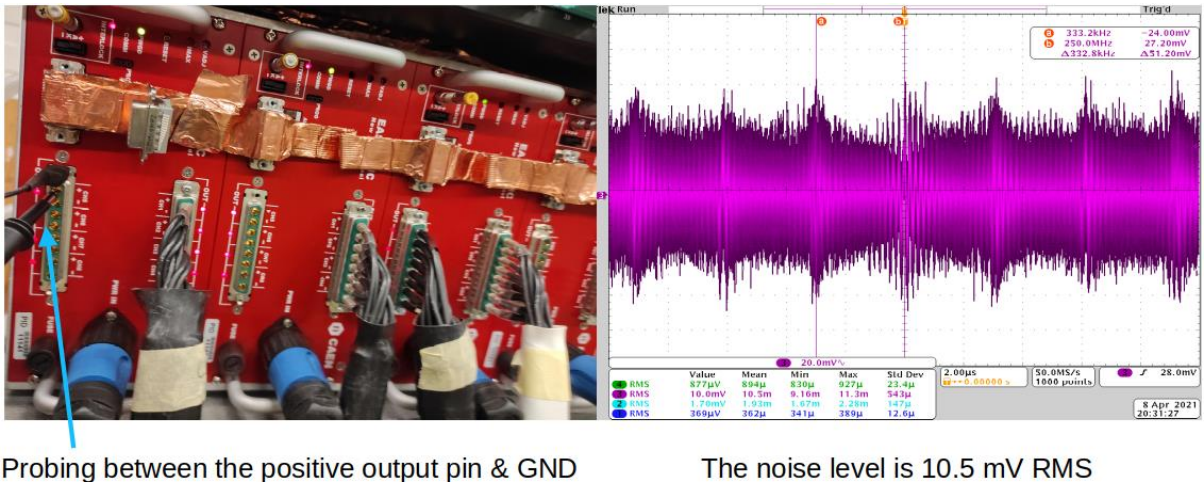


Figure 59: Noise measurement of one ICS channel before any modification.

These findings were debated in the Task Force's internal meetings, and the Head asked for a more profound investigation to prove that the ICS noise affects the detector. For this, the noise of the ICS had to be reduced, and then compare the noise baselines

In order to reduce the noise, a set of capacitors was used to provide a path of least resistance to the ground. As a first attempt, one 1μF capacitor in parallel with one 0.1μF was connected between the plus of the ICS output to the ground (similarly, the same configuration was used for the minus-return pin), as seen in Figure 60.

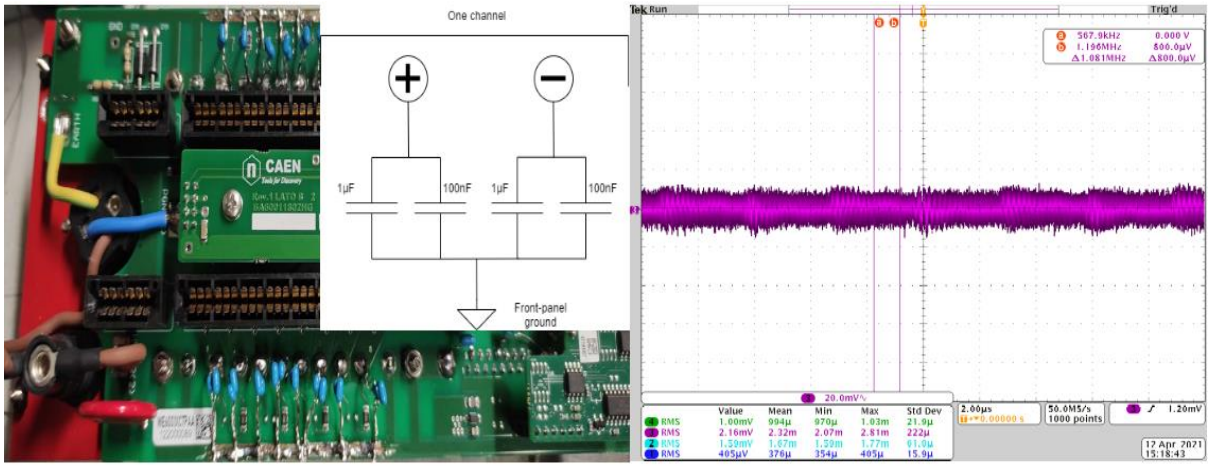


Figure 60: Left: A modified ICS front panel with 1μF in parallel with 100nF to ground. Right: Noise level measurement after the modification with 1μF and 100nF capacitors in parallel. The noise level is now at 2.32mV RMS, reduced by a factor of five.

The selection of those capacitors was not optimal (they were the only ones available at that time). However, the resonance frequency of the through-hole 1μF capacitor was close to 5MHz. Although the above solution was not optimum, the noise level dropped by a factor of five. This modification was applied in a kind of crude manner to all 32 channels so that an entire MM sector could be tested.

Despite the claims that this modification would not offer significant improvement, we managed to do a noise baseline run, and the noise improvement was significant Figure 61). More detailed plots showing the difference with and without the ICS modification can be found in Figure 84 in the Figures appendix. It is worth mentioning that this improvement concerns a MM sector where all possible ground modifications failed.

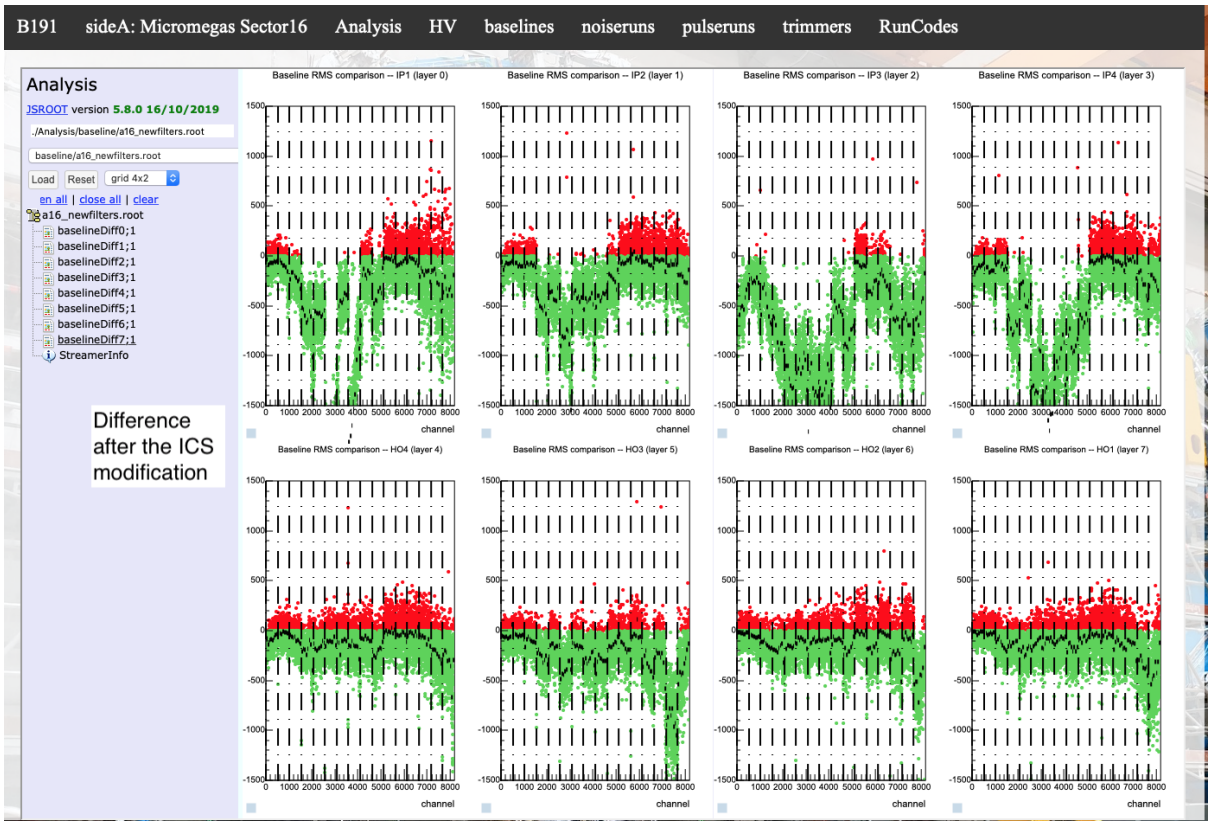


Figure 61. Noise baseline comparison before and after the ICS modification. The green (red) color corresponds to noise reduction (increase), and the black trcae is the overall result. The black trace indicates that there is no increase; in the worst case, there is no difference between the runs (the shown increase in the noise is due to low statistics samples).

The above results were presented in the Task Force internal meetings, where it was decided that the ICS modification is mandatory. The following paragraphs describe the procedure for identifying the optimal capacitors' configuration and their optimal placement in the ICS front panel.

To find the optimal capacitor values, many simulations (using the LTSpice) were performed using capacitor models from the manufacturers. It was found that three capacitors are needed for every output to provide a more broadband filter since the final cabling scheme in the experiment would probably cause the noise frequency to shift. The final values for through-hole capacitors are 1μF in parallel with 680nF in parallel with 470nF. According to the simulations (Figure 63) the impedance of the three capacitors at 5MHz is ~29mΩ, while the 1μF in parallel with 100nF configuration provides 215mΩ impedance at the same frequency (Figure 62).

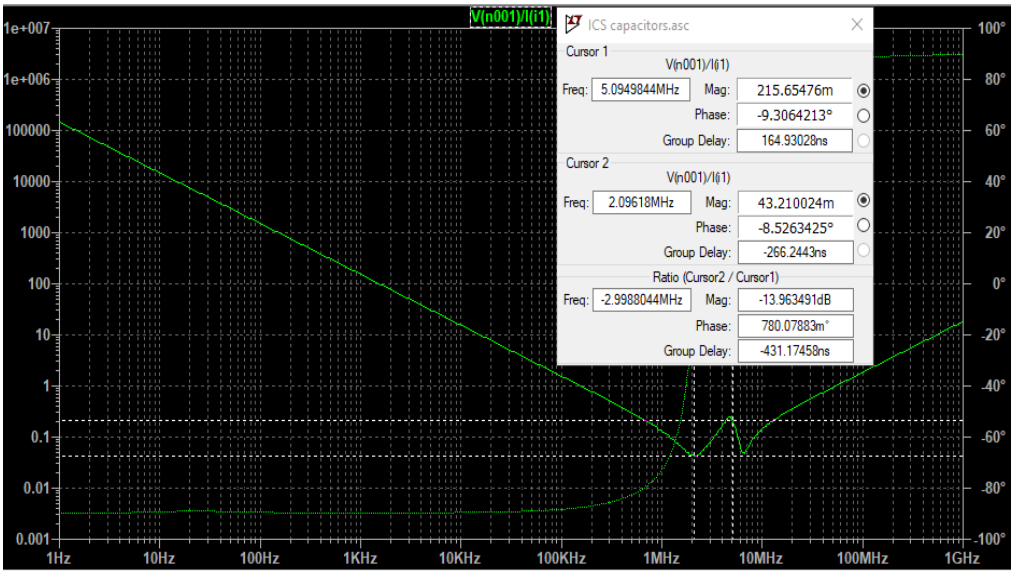


Figure 62: Simulation of 1μF in parallel 100nF. This configuration is not optimal since the anti-resonance of the 100nF capacitor results in high impedance at 5MHz

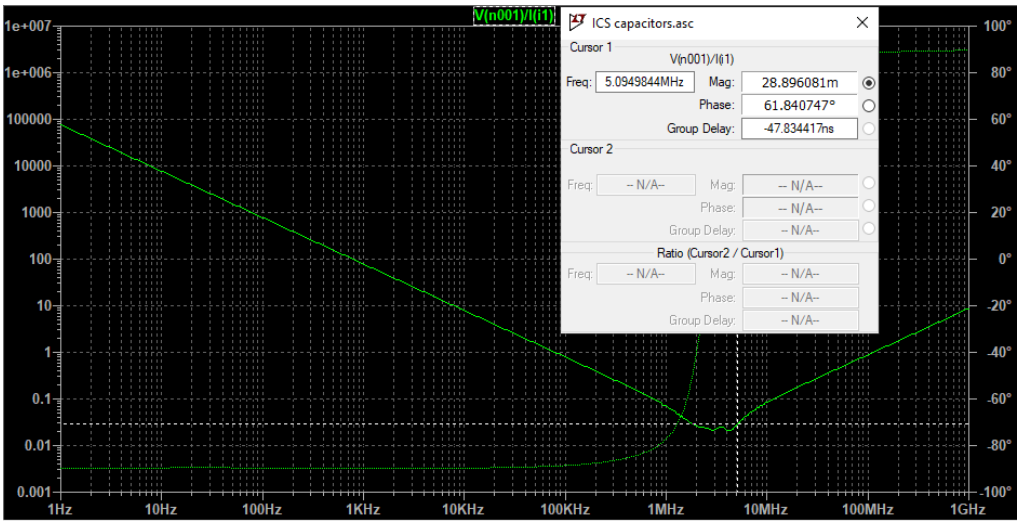


Figure 63: Simulation of the 1μF parallel with a 680nF and a 470nF capacitor filter. As seen in cursor measurement window the impedance at 5MHz is ~28mΩ.

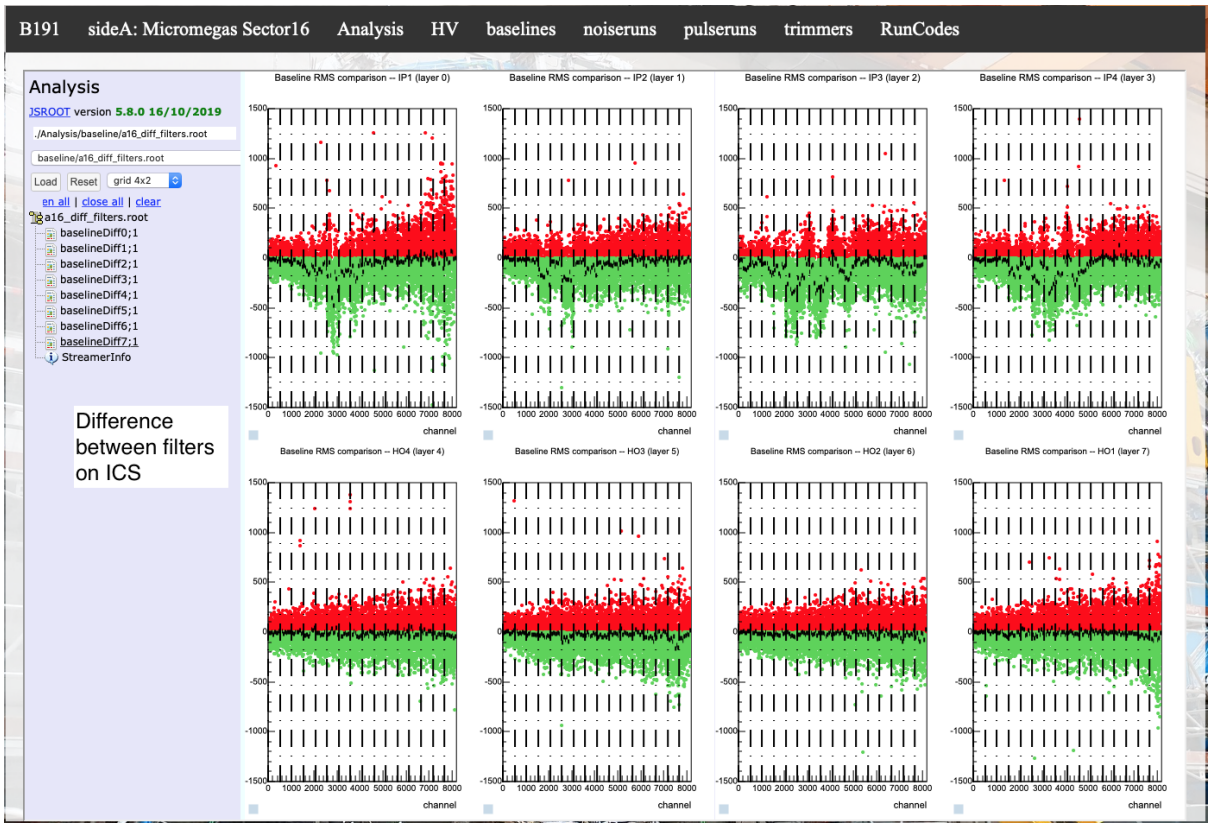


Figure 64: Noise baseline showing the difference between the two filters. There is a slight improvement, but the main goal of the three-capacitor filter is to provide a more broadband filter.

The three capacitors' configuration reduced the noise by a factor of ten, from 10.5mV RMS noise (without the capacitors) to 1.31mV RMS. Moreover, this filter has an impedance of less than 100mΩ in the 1MHz to 10MHz range.

The next problem to solve is how to mount all these capacitors (48 capacitors, three capacitors × eight channels × two pins) to ICS front panel. One solution is to mount them, as shown before, by scratching the silkscreen of the PCB and soldering them in place, as shown on the left side of Figure 65. A more elegant solution to this problem was proposed instead by the author of this thesis; to fabricate a small mezzanine board where SMD capacitors are soldered. The board could be easily mounted to existing screws and soldered to the output pins of the ICS, as shown in the right part of Figure 65.

More simulation figures can be found in the Appendix (Figure 82, Figure 82, Figure 83 and Figure 84).

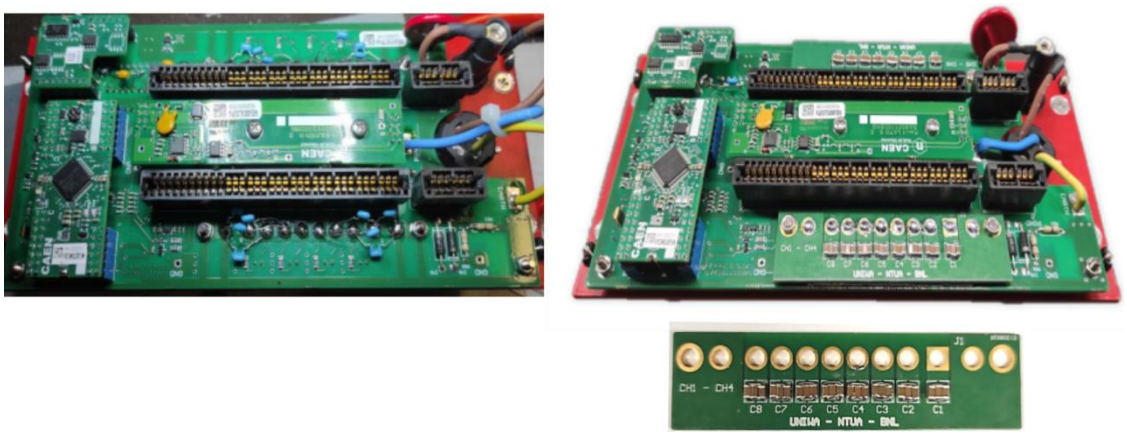


Figure 65: Comparison of the two solutions for the filter placement on the ICS. Left: soldering one 1μF capacitor (proposed by the ICS person in charge). Right: a mezzanine card with three SMD capacitors (proposed and developed by the author of this thesis)

Since the SMD capacitor has different dimensions and no leads, new simulations had to be performed to find a set of three capacitors with the same response (or even better) as the through-hole ones.

The new set of capacitors consists of a 2.2μF capacitor parallel with a 1.5μF and a 1μF capacitors. The performance of this capacitor bank is slightly better than the through-hole counterparts, with an impedance of 10mΩ 5MHz. The noise comparison plot of the two capacitor types through–hole and SMD is shown in Figure 66.

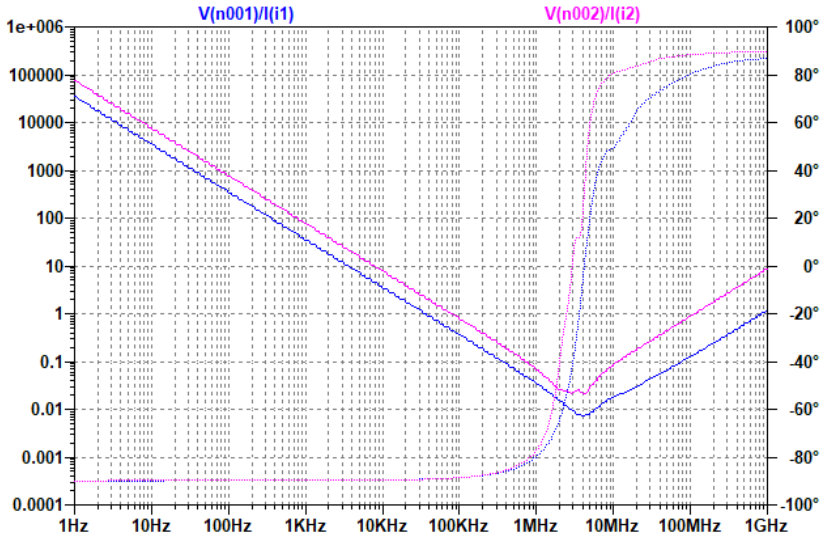


Figure 66: Simulation–comparison of the impedance between the through-hole filter (magenta) and the SMD counterpart (blue).

The noise comparison plot of the two capacitor types and without them is shown in Figure *67.*

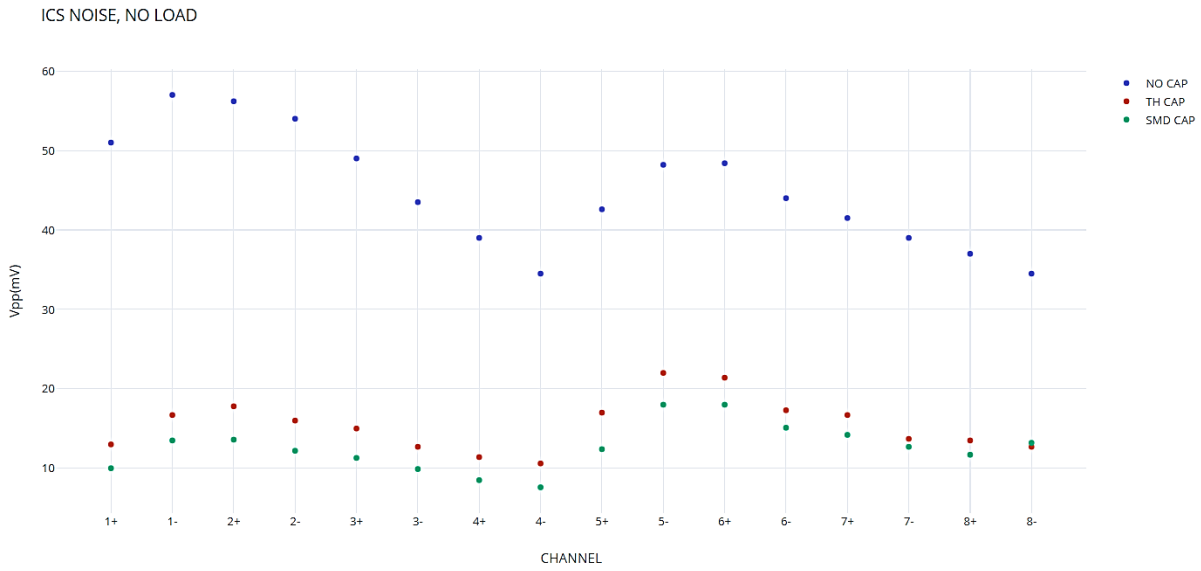


Figure 67: ICS noise level comparison (Vpp(mV)) without load. Blue trace: unmodified ICS. Red trace: with through-hole 1μF||680nF||470nF capacitors. Green trace: with the mezzanine board hosting 2.2μF||1.5μF||1μF SMD capacitors.

Despite the fact that the solution of the mezzanine board with the SMD capacitor had better performance and provided a cleaner and easier solution to apply and maintain, initially there was a claim by the ICS team, that the mezzanine board may introduce destructive mechanical stress to the ICS PCB, that prevented the use of the method for the ICSes of the NSW Side-A. However, since no evidence of such mechanical stresses was found, the Task Force experts decided to place the mezzanine boards to the ICSes of the Side-C NSW and to the spare ones.

It is worth mentioning that this mezzanine board is the first ever board carrying the UNIWA logo used in a high-energy physics experiment and that the noise reduction followed by the ICS modification described in this subsection gave the green light for the installation of the NSW detector in the ATLAS experiment on time

5.5 MMFE8 boards Repairs and testing

Close to the end of the NSW integration, another big problem appeared. Many MMFE8 front-end boards were failing at an alarming rate. Although there were provisions for spares, the number of failed boards exceeded the number of spares. Many types of failure were identified, such as ASIC failures (VMM, SCA, ROC, and FEAST), shorted capacitors, and damages during the integration process. Most of the failures, though, were related to the VMM ASICs. The problem was narrowed down to the last VMM batch that was fabricated. These VMMs, due to an error of the manufacturer, were fabricated with a 0.1mm thinner BGA-400 package than normal. This fact resulted in a deformation of the VMM package, creating stress on the BGA soldering. Thus, some of the VMM's pin pads could be detached from the PCB of the MMFE8. The bending analysis from G. Iakovidis is shown in Figure 68.

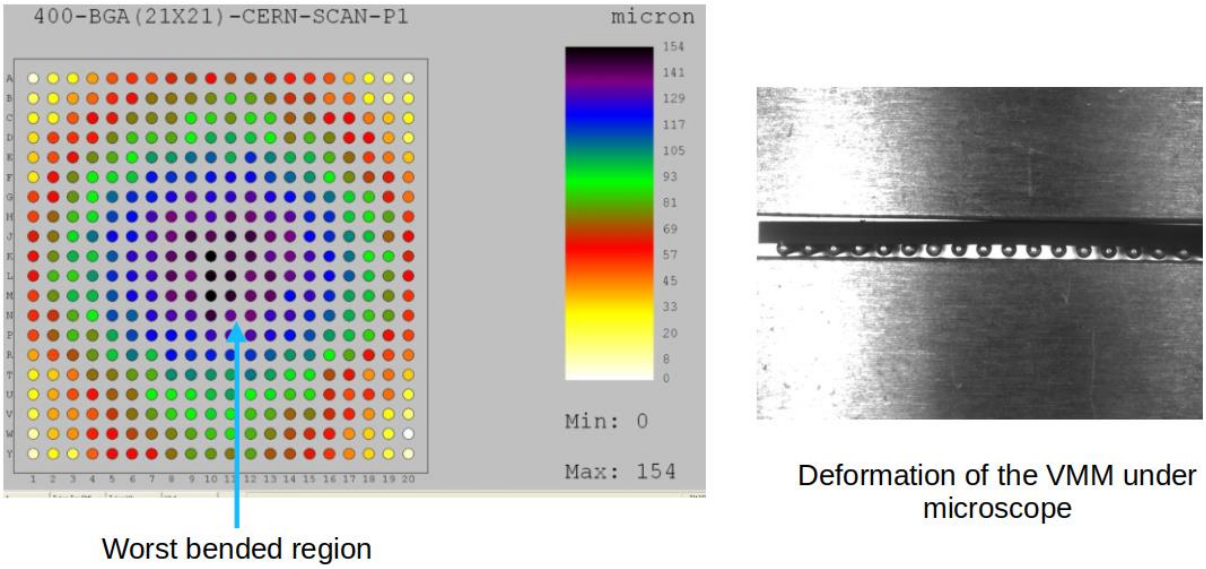


Figure 68: Bending of the VMM ASIC.

Given the tight time constraints of the project, there was a high risk that side C of the NSW would not be ready on time, meaning that it would not be installed until the next LHC shutdown in 2026. Thus, the immediate repair of the MMFE8s became the priority of the NSW project. The CERN's SMD Lab was responsible for performing these repairs (mostly the replacement of VMM), but the replacement cost was high (100CHF per chip), and most importantly, they could deliver only 2-3 boards daily. To reduce the project's cost and, most significantly, the delay in the accomplishment of the NSW integration, the author volunteered to perform the fault detection and the replacements by hand, despite the small form factor of the VMMs (BGA-400 with 1 mm pitch). Up to 50 boards per day were repaired, with more than 50 components replaced.

The repair procedure mandated that the boards had to be tested on a bench using the Arizona MMFE8 setup, which was able to perform a series of tests. Then, the boards had to be repaired and retested before being integrated into the MM sectors.

One of the MMFE8 tests was a noise baseline run. However, this test needed ten minutes to complete, creating a bottleneck in the repair procedure. To reduce the baseline tests' duration, a new setup was developed using the same hardware as at the L1DDC testing. Accordingly, new firmware (Figure 69) and software (Figure 70) were developed based on the L1DDC testing (described in Chapter 4). The new setup could take 1000 samples per VMM channel (64 channels×8 VMMs×1000 samples=512000 samples) in less than a minute (a factor of ten reduction).

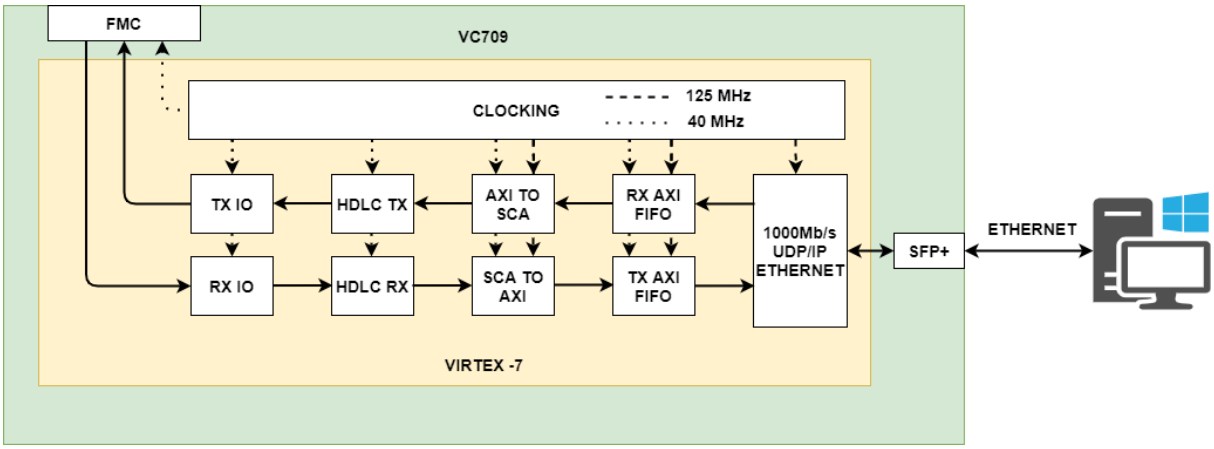


Figure 69. Top: The block diagram of the firmware showing the 1Gb/s Ethernet, the RX/TX FIFOS, the SCA-to-AXI/AXI-to-SCA bridge, the SCA HDLC module, and the TX/RX logic.

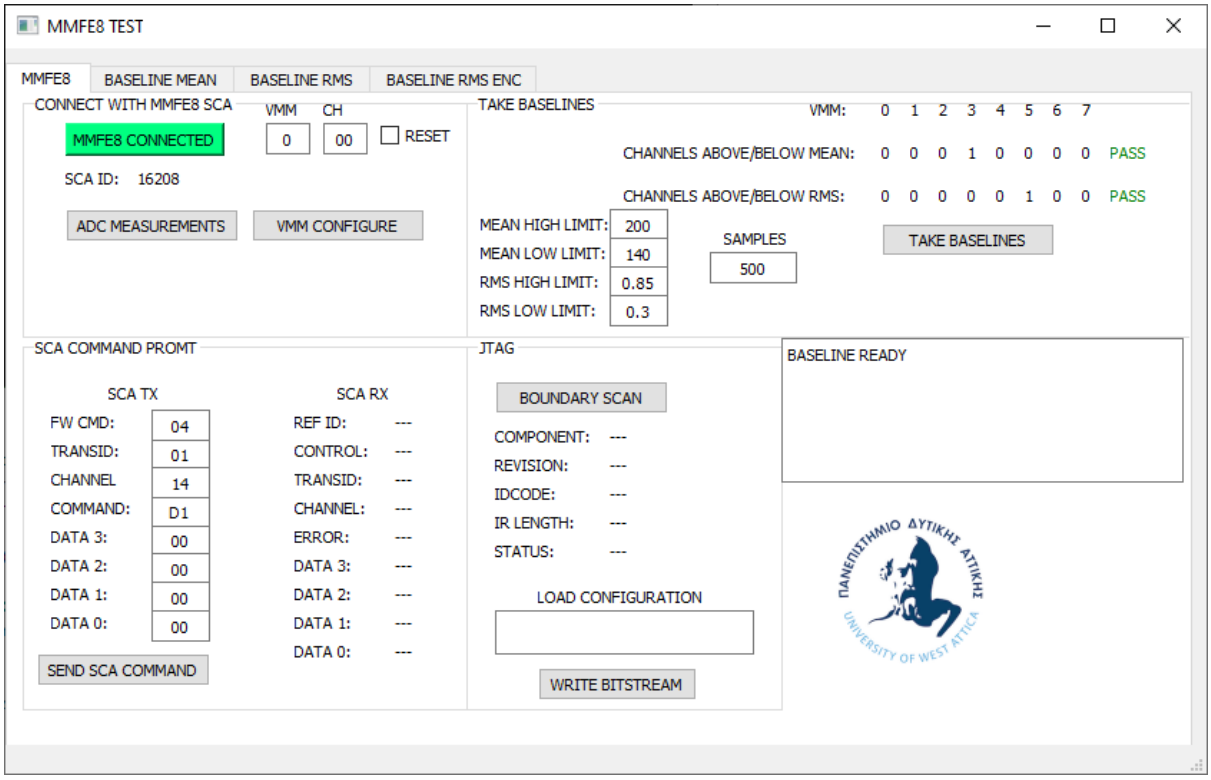


Figure 70: The GUI front panel with the various settings and functions.

The firmware of the MMFE8 testing consists of a) the open source 1Gb/s UDP/IP Ethernet core, described in section 4.2.4, b) an SCA to AXI bus bridge (and vice versa) with an AXI bus FIFO for the connection with the Ethernet. At the same time, the other end of the bridge is connected to the HDLC module, which implements the SCA communication protocol. Finally, the 2-bit at 40MHz (80Mb/s) data stream from the HDLC module is serialized/deserialized from the TX and RX logic, respectively.

The software part of the MMFE8 tester was developed in C++ using the Qt IDE. The software implementation has a UDP/IP connection with the firmware. This communication can send configuration data to the firmware and subsequently to the SCA of the MMFE8. On the other hand, it can receive the replies of the SCA. The procedure to take a baseline run is as

follows: In the beginning, the software configures the SCA and the ROC ASICs of the MMFE8. Then one by one, the VMMs are configured by SCA's Serial Peripheral Interface (SPI), so the analog signal of one of the VMM's 64 channels is driven to the Peak Detect Output (PDO) pin. The PDO pin of every VMM is connected to the SCA's ADC input pins (eight ADC inputs, one for every VMM). The software then reads and stores the value sampled by the ADC; this operation is repeated for the number of samples we have chosen in the UI. After finishing the first VMM channel, the VMM is configured again, so the second channel is driven to the PDO, and the sample cycle starts again; this operation is performed for all 64 channels. Finally, all the previous procedures were repeated for every VMM. Using the data samples, the mean value in mV of every VMM channel is calculated using Equation (1), where x_i is a sample of a given VMM channel, and N is the total number of samples.

$$Mean(mV) = \mu = \frac{\sum_{i=1}^{N} x_i}{N}$$

Equation (1)

The σ of the channel's noise distribution is calculated using Equation (2).

$$RMS(mV) = \sigma = \sqrt{\frac{\sum_{i=1}^{N}(x_i - \mu)^2}{N}}$$

Equation (2)

The σ expressed in Electron Noise Charge (ENC) is calculated using Equation (3), where G is the gain setting of VMM's amplifier.

$$RMS\ ENC = \frac{RMS(mV)}{G(^{mV}/_{fC})} = \left(\frac{RMS}{9} \times 6240\right) e^{-}$$

Equation (3)

All the calculated values are then plotted in three different plots; for example, the RMS(mV) is shown in Figure 71.

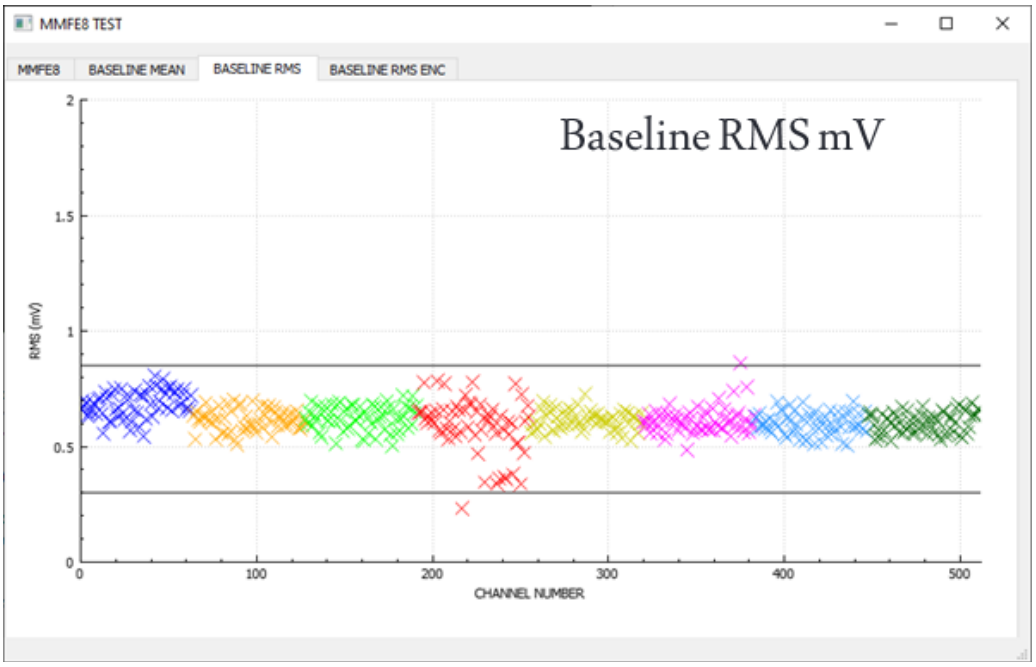


Figure 71: MMFE8 noise baseline, using the MMFE8 test setup. Different colors are used for every VMM.

For plotting, the open-source QCustomplot library is used. Moreover, for every plot, two limits are applied: the upper and the lower. The upper limit indicates whether a VMM channel is "noisy," while the lower indicates a "dead" channel. These limits provide the user with a fast way to validate the functionality of the MMFE8 board under test. The values of the limits are set by the user in the GUI depending on whether the MMFE8 is tested on the bench or on the detector. The limits are different for every PCB of the detector since the PCBs with longer strips will have higher baseline noise.

Conclusion

This master thesis was carried out under a contract awarded by the ATLAS collaboration for contributing to the challenge of installing the NSW at the ATLAS detector on schedule.

Initially, the scope of the thesis was to contribute to developing a test setup (hardware, firmware, software) to evaluate the performance of the L1DDC boards responsible for the readout and the data transfer of the NSW Micromegas detectors. Four identical test stations have been implemented at the University of West Attica (UNIWA), the National Kapodistrian University of Athens (NKUA), the National Centre for Scientific Research (NCSR Demokritos), and CERN. In total, the performance of 572 MM-L1DDCs (522 production boards and 50 pre-production boards), 572 sTGC-L1DDCs (522 production boards and 50 pre-production boards) together with 40 RIM-L1DDCs has been evaluated, and faults have been repaired (Chapter 3).

During this master thesis grant at CERN, the NSW project fell well behind schedule because of critical problems. Besides, the COVID-19 pandemic resulted in the postponement of all CERN activities, which caused additional backlogs. Thus, the need to contribute to many new issues arose alongside developing the L1DDCs' test station.

Consequently, the objective of the thesis was broadened to include solving problems encountered during the integration of the Micromegas electronics into the NSW detector (before its installation in the wheel frame). Thus, this thesis contributed significantly to developing hardware, software, and firmware to address the problems that had emerged. In particular, the following off-detector boards have been developed:

- The Clock Distribution Board which distributes low jitter 160 MHz clocks to the Rim electronics through the Rim-L1DDC (section 5.1)
- The LVDS to TTL adapter board for the validation of Micromegas wedges with cosmic rays (section 5.2)
- The Differential Safety Mechanism for protecting the detector wedges against sudden increases in the static gauge pressure inside its volume (section 5.3).

Furthermore, this thesis contributed significantly to solving the severe noise issues that emerged while integrating the NSW detector' electronics. The noise problem was critical to be solved urgently for the NSW detector to be installed on the wheel on time. In this thesis, noise sources were identified and suppressed, and the grounding scheme of the detector was improved, providing the best possible noise reduction. Specifically, to resolve the noise problem, the following actions have been performed in the framework of this thesis:

- Identify the ADDC board as a noise source (due to an error in its design). Develop and evaluate ten prototype Faraday cages to reduce the noise of ADDC boards. Fabrication, installation, and evaluation of 550 Faraday cages (section 5.4.1).
- Identify choke points in the ground plane of the MM PCBs and weak connections between different PCBs as noise sources and improvement of the grounding scheme of the MM detectors (section 5.4.2)
- Identify the ICS power supplies that power all the on-detector electronics as the primary source of the noise. A filter has been designed and implemented by a mezzanine board at the

ICS power supplies' front panels that significantly reduced the noise, giving the green light for installing the NSW detector in the ATLAS experiment on time. The mezzanine boards carry the UNIWA logo have been installed and used for reducing the noise of the Side-C NSW detector (section 5.4.3).

Additionally, various repairs have been performed on the MM detectors' front-end boards (MMFE8) that were failing to function at an alarming rate. For the testing of the MMFE8 boards' noise levels, given the tight time constraints of the project, a new test bench (firmware and software) has been developed, which was about three times faster than the available one (section 5.5).

Publications in Scientific Journals

[I] T. Alexopoulos, T. Geralis, P. Gkountoumis, L. Levinson, I. Mesolongitis and O. Zormpa. Ultra-low jitter clock distribution for the trigger electronics of the New Small Wheel for the ATLAS experiment. Journal of Instrumentation, Volume 17, May 2022.

Publications at International Conferences

[II] P. Gkountoumis, D. Matakias, I.P. Mesolongits, E. Politis, et al. Validation of the Production-Phase Level-1 DataDriver Cards for the Readout and Trigger System of the ATLAS New Small Wheel Detector. MOCAST, 07-09 September 2020

[III] T. Alexopoulos, E. N. Gazis S. Maltezos, and I. Mesolongitis. Design of a Differential Safety Mechanism (DSM) Dedicated to the NSW Micromegas Wedges. Journal of Physics: Conference Series. HEP 2021.

Internal publications in ATLAS experiment (ATLAS NOTES)

[IV] T. Alexopoulos, E. N. Gazis S. Maltezos, and I. Mesolongitis. Design of a Differential Safety Mechanism (DSM) Dedicated to the NSW Micromegas Wedges. ATLAS NOTE. April 2021.

[V] T. Geralis, et. al, The Serial and LVDS repeaters for the ATLAS New Small Wheel sTGC trigger. ATLAS NOTE, November 2022.

ATLAS weekly meetings

Indicative presentations/contributions:

A. NSW weekly General meetings

Ioannis Mesolongitis, Update on MM electronics refurbishment, https://indico.cern.ch/event/1064690/, 07-08-2022

B. NSW Integration weekly meetings

Theo Alexopoulos, George Iakovidis, Giannis Mesologitis, BB5 progress report, https://indico.cern.ch/event/1020099/, 19.03.2021

C. **NSW Noise Task Force Meetings**

- George Iakovidis, Theo Alexopoulos, Giannis Mesolongitis, Noise inspection, https://indico.cern.ch/event/1021452/, 24.03.2021
- George Iakovidis, Theo Alexopoulos, Giannis Mesolongitis, Noise inspection, https://indico.cern.ch/event/1023149, 31.03.2021
- Theo Alexopoulos, George Iakovidis, Giannis Mesolongitis, MM Noise Investigation and Evolution in BB5/B191, https://indico.cern.ch/event/1024792/, 07.04.2021.
- Theo Alexopoulos, George Iakovidis, Giannis Mesolongitis, MM Noise Investigation and Evolution in BB5/B191 BB5 progress report, https://indico.cern.ch/event/1026813/, 09.04.2021
- George Iakovidis, Theo Alexopoulos, Giannis Mesolongitis, Noise inspection, https://indico.cern.ch/event/1034051/, 30-04.2021

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Figure 72: A large MM sector during the installation of electronics.

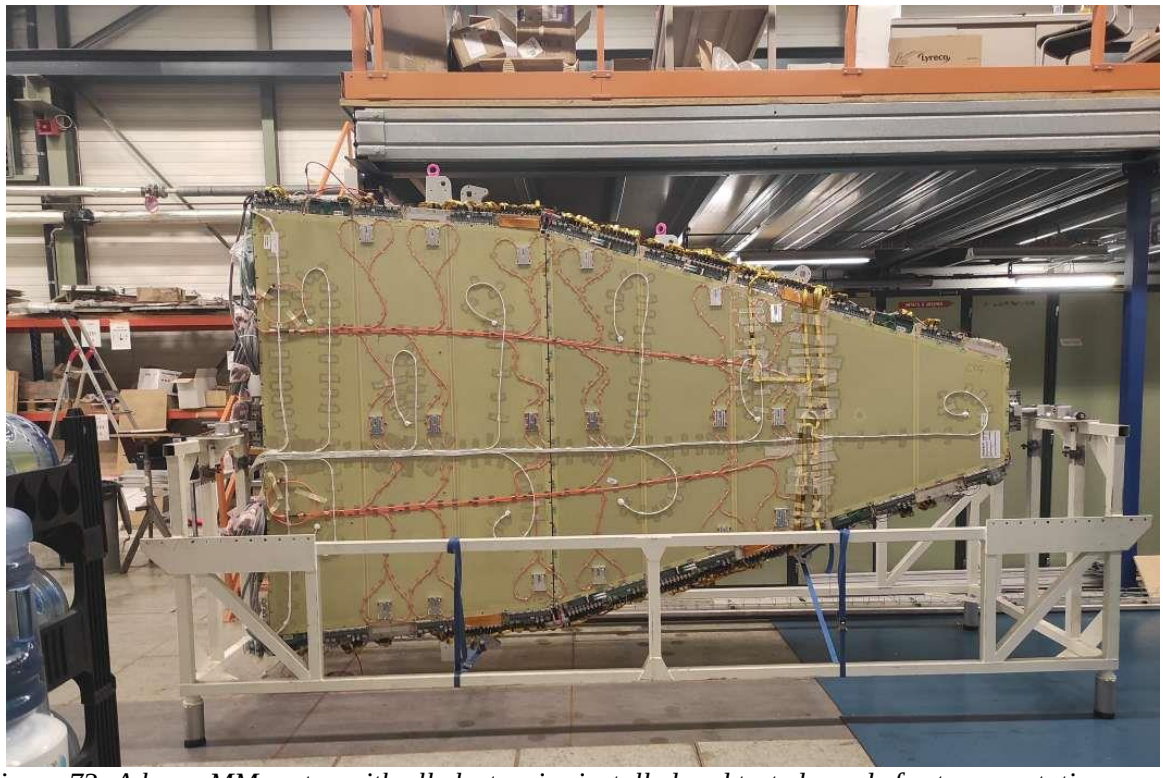

Figure 73: A large MM sector with all electronics installed and tested, ready for transportation.

Figure 74: A small sTGC wedge with all electronics installed.

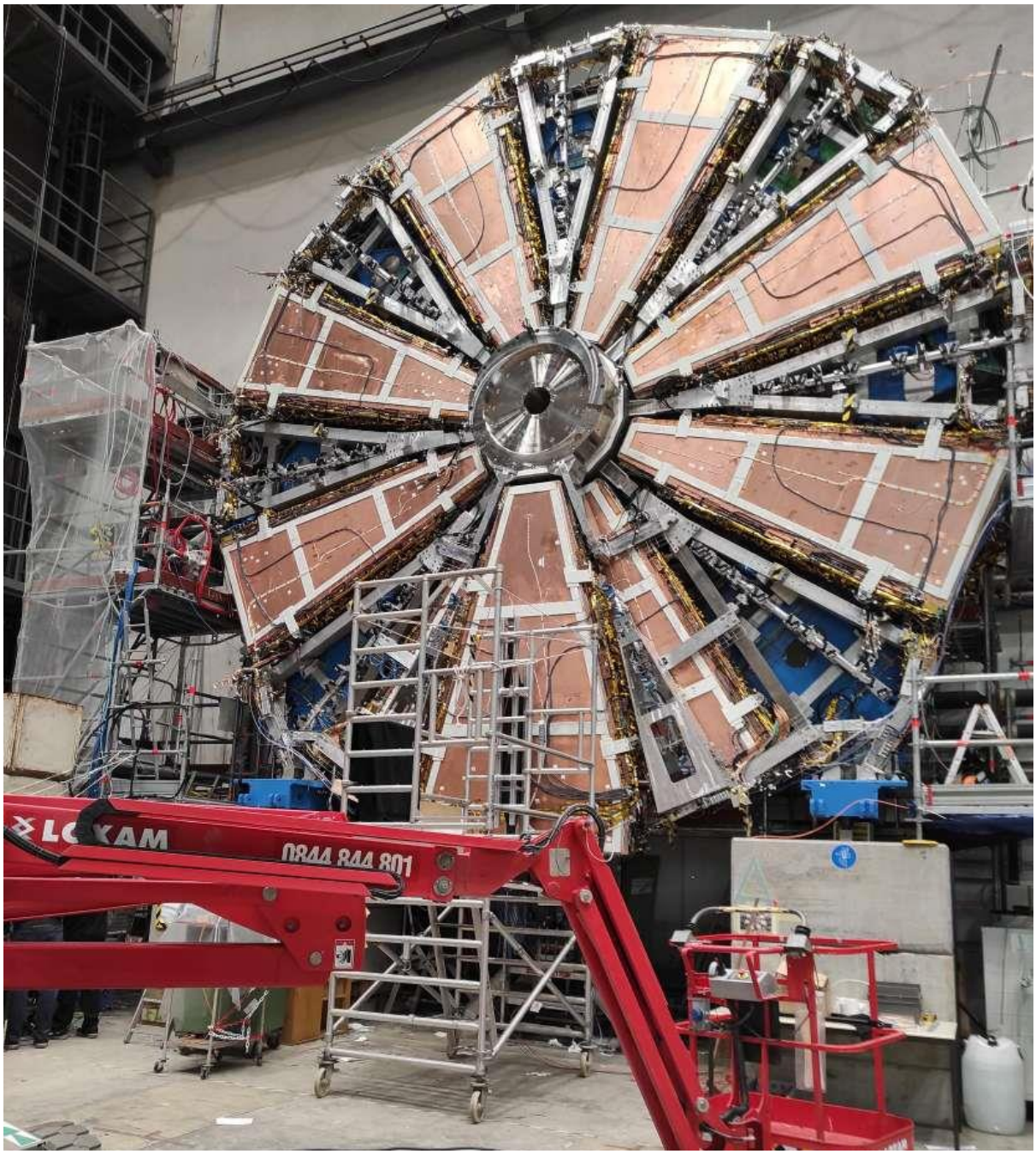

Figure 75: NSW side A with all small sectors installed plus one large sector at the bottom.

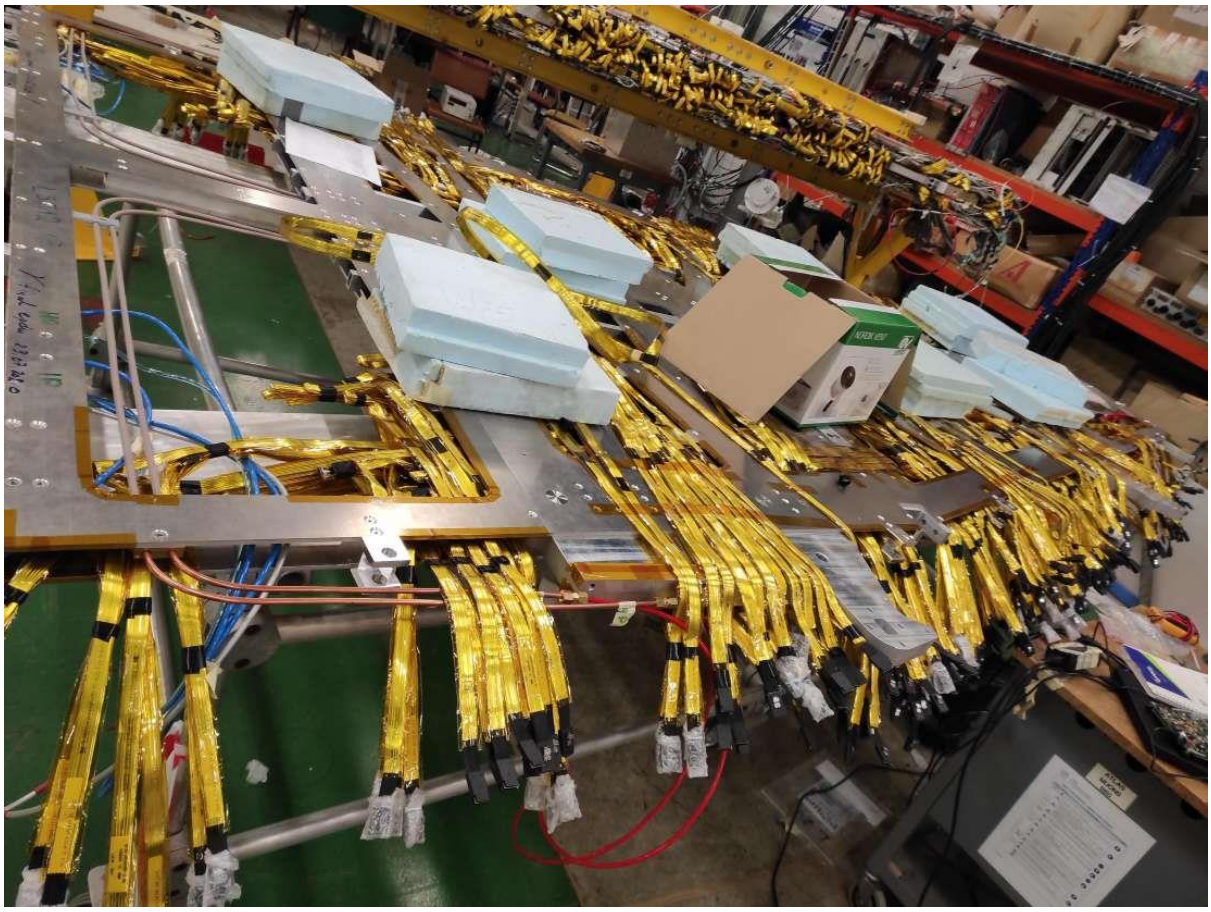

Figure 76: MM spacer frame with all miniSAS cables in place.

Figure 77: ADDC Faraday cage manufactured by a company and soldered manually.

Figure 78: Spectrum of the ICS noise picked up by the loop antenna. The noise peaks at 5MHz when the ICS is powered on and vanishes when the ICS is off.

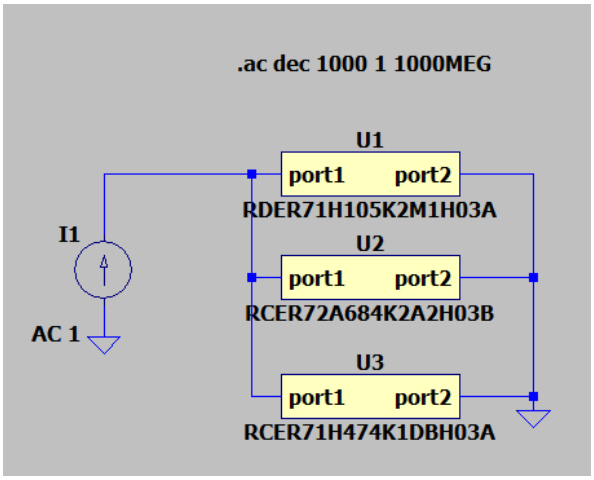

Figure 79: Schematic of the capacitor filter for the simulation using the LTSpice.

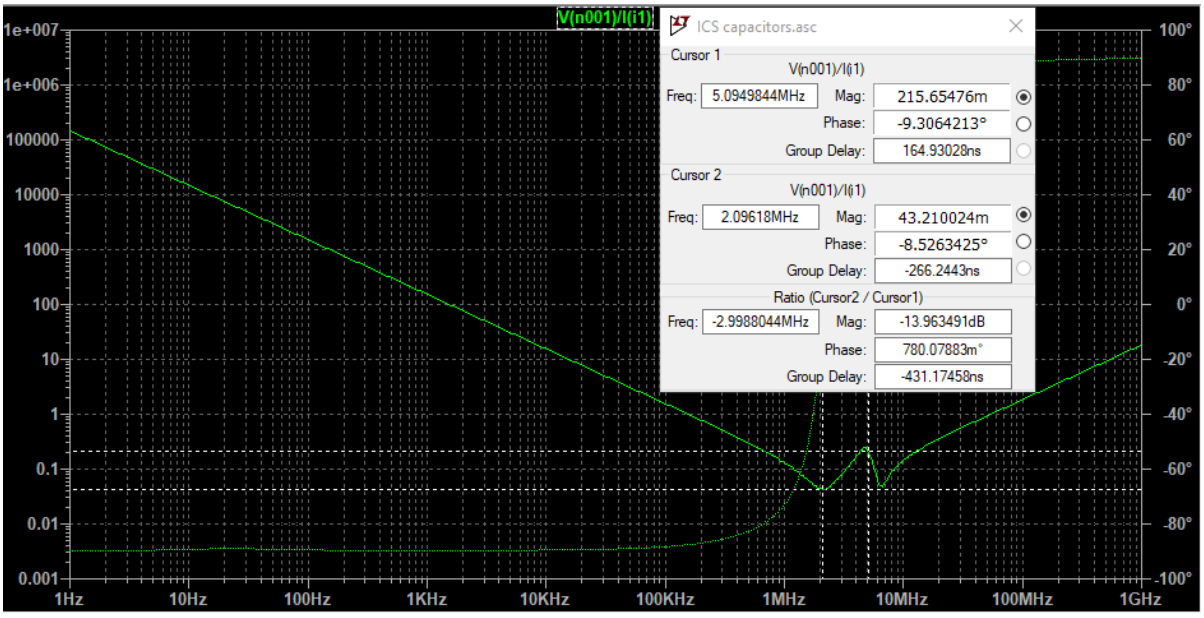

Figure 80: Simulation of 1μF in parallel 100nF. This configuration is not optimal since the anti-resonance of the 100nF capacitor results in high impedance at 5MHz.

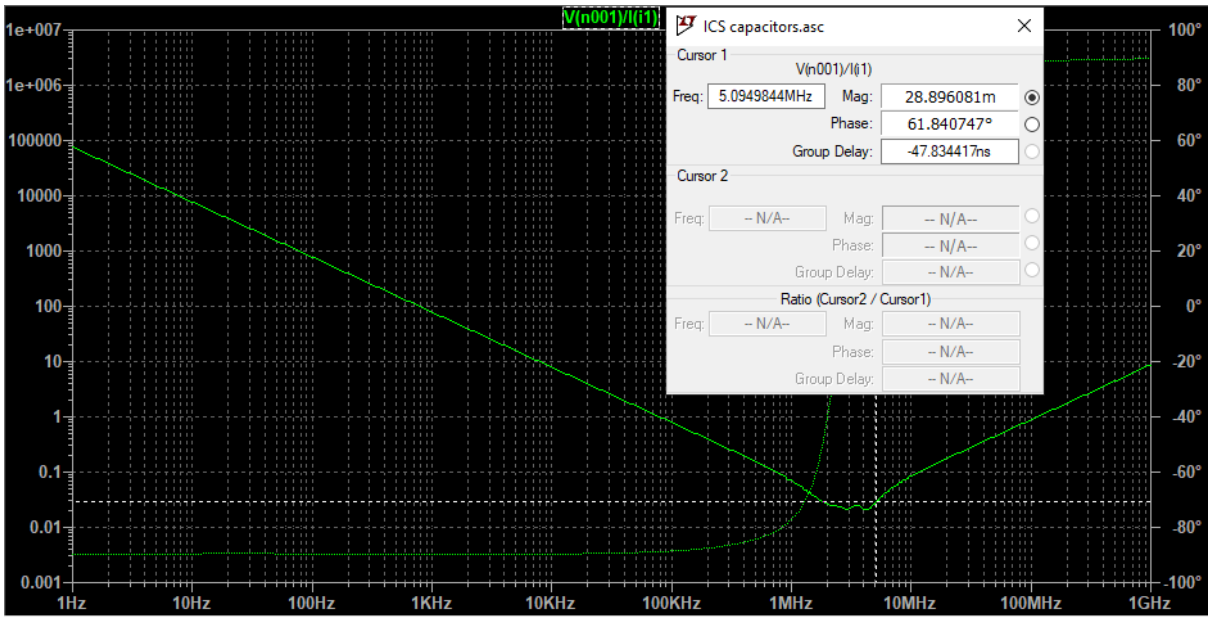

Figure 81: Simulation of 1μF||680nF||470nF through-hole capacitors. This configuration results in low impedance, about 29mΩ at 5MHz.

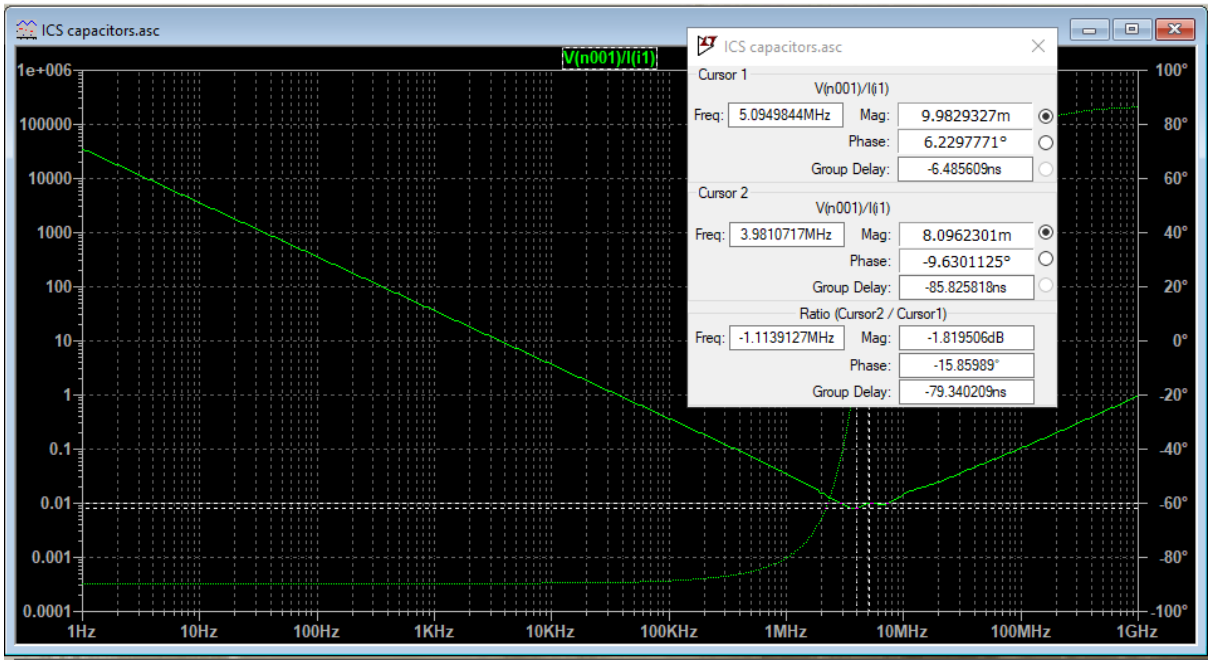

Figure 82: Simulation of 2.2μF||1.5μF||1μF SMD capacitors which result in 10mΩ impedance at 5MHz.

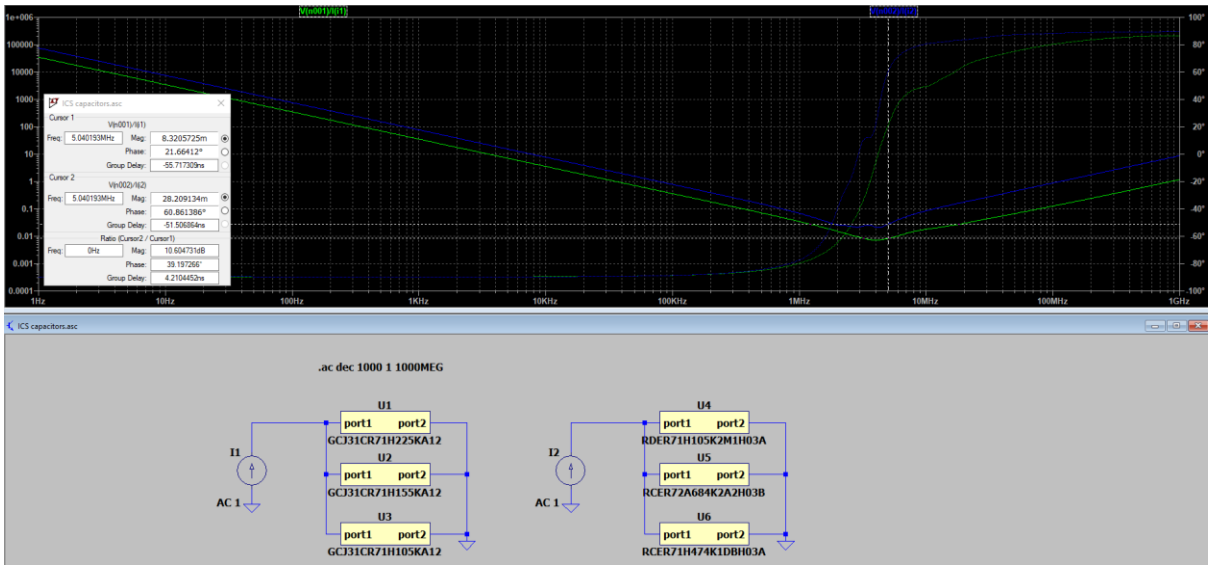

Figure 83: Comparison of the through-hole and SMD capacitor filter. The blue trace is the through-hole filter, and the trace is the SMD one.

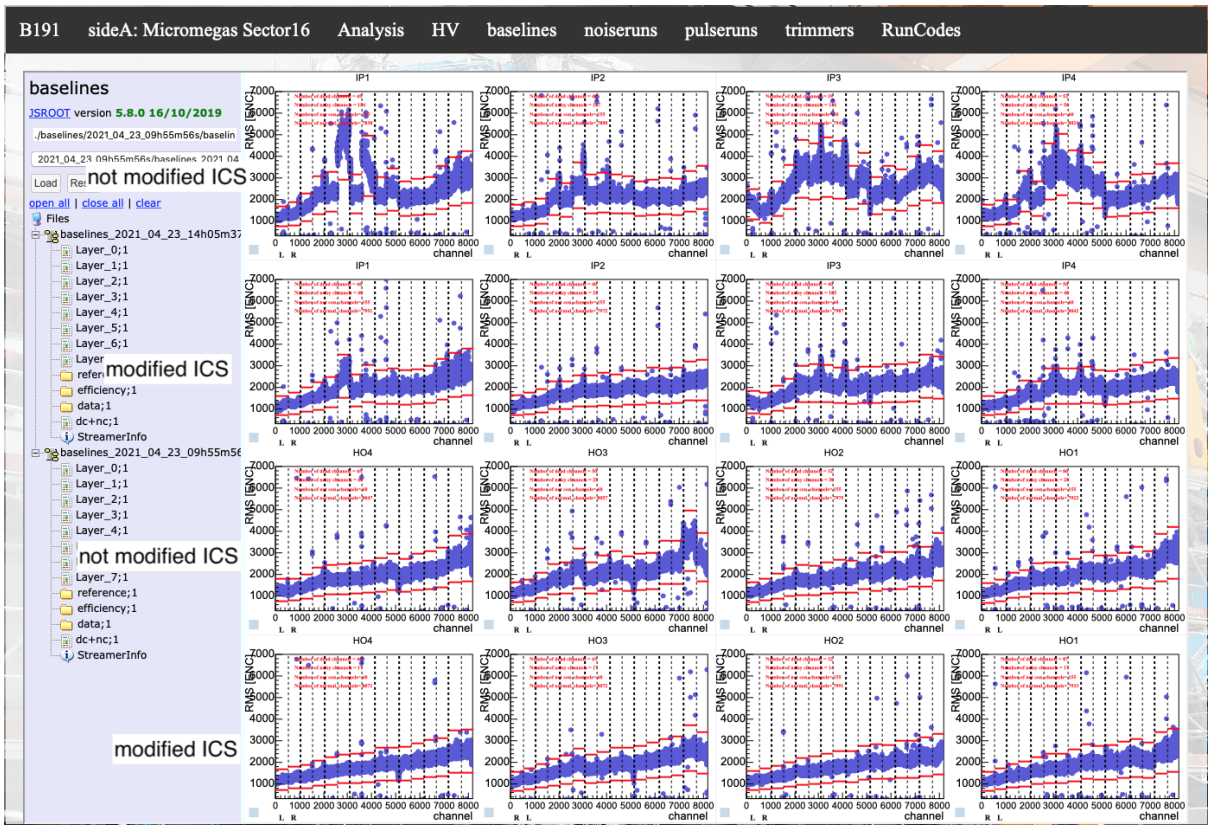

Figure 84: Noise baseline comparison without and with the ICS modification.

Code Appendix

[I] sTGC-L1DDC test firmware.

[II] Rim-L1DDC test firmware.

[III] MM-L1DDC test software.

[IV] sTGC-L1DDC test software.

[V] Rim-L1DDC test software.

[VI] MM cable testing firmware.

[VII] Clock distributor software.

[VIII] MMFE8 test firmware for MMFE8 Artix-7.

[IX] MMFE8 test firmware for VC709.

[X] MMFE8 test software.